# SigmaDSP™ Multichannel Audio Processor With Embedded 2ADC/8DAC Codec

Preliminary Technical Data

# ADAU1421

## FEATURES

**Fully programmable Audio DSP for enhanced sound processing**
**Features SigmaStudio, a proprietary Graphical Programming Tool for fast development of custom signal flows**
**Easy implementation of 3rd party Audio Algorithms**
**Scalable digital audio delay line**
  **Pool of 400ms (for example 200ms for stereo channel)**
**High performance integrated ADCs and DACs**
**100dB Dynamic Range, -95dB THD+N**
  **1 stereo analog input (ADC)**
  **4 stereo analog inputs w. MUX to stereo ADC**
  **4 stereo (8-ch) analog outputs (DACs)**
**Dedicated Headphone output with integrated Amplifier**
**Multi-channel digital I/O**
  **8-channel I²S input and output modes**
  **8-and 16 channel TDM input and output modes**
  **2-channel (1-stereo) asynchronous I²S input with integrated up-converting Sample Rate Converter, supporting sample rates from 5kHz to 50kHz**
**I²C control interface**
**Operates from 3.3V (Analog), 1.8V (Digital Core), 3.3V (Digital Interface)**
**Features on-chip regulator for single 3.3V operation**
**80-lead LQFP Package (12x12mm)**
**Temperature Range: -40C to +105C**

## APPLICATIONS

**Automotive Audio Processing**
  **Car Radios**
  **Navigation Systems**
  **Rear-Seat Enterainment Systems**
  **DSP Amplifiers (Sound-System Amplifiers)**
**Commercial Audio Processing**

## PRODUCT OVERVIEW

The ADAU1421 is an enhanced Audio Processor. Integrating high performance analog and digital I/O with a powerful audio specific programmable core enables designers to differentiate their products through audio performance.

## FUNCTIONAL BLOCK DIAGRAM

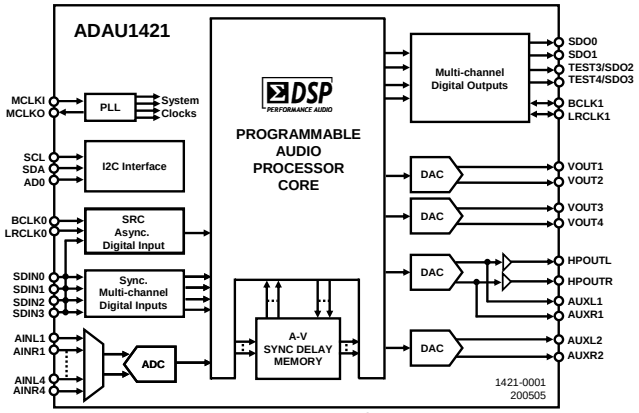


*Figure 1. 80-Lead LQFP*

The audio processing core is based on ADI's SigmaDSP™ technology featuring full 28-bit processing (56-bit in double precision mode), a sophisticated fully programmable dynamics processor and delay memory.

This allows the system designer to compensate for the real-world limitations of speakers, amplifiers and listening environment, resulting in a dramatic improvement of the perceived audio quality through speaker equalization, multi-band compression/limiting and 3rd party branded algorithms.

The analog I/O integrates ADI's proprietary Continuous Time Multi-bit Sigma-Delta architecture in order to bring a higher level of performance to systems required by 3rd party algorithm providers in order to meet system branding certification. The analog inputs feature a 100dB DNR ADC fed from a 4 stereo input MUX. The main speaker outputs can be supplied as a voltage output from the integrated 100dB DNR DAC channels. Also available is a dedicated headphone DAC with integrated amplifiers and additional auxiliary analog outputs.

The ADAU1421 supports multi-channel digital inputs and outputs. An integrated Sample Rate Converter (SRC) on one channel provides the capability to support any input sample rates in the range from 5kHz to 50kHz synchronizing this input to the internal DSP engine.

The ADAU1421 is supported by a powerful graphical programming tool which includes blocks such as general filters, EQ filters, dynamics processing, mixers, volume and 3rd party algorithms for fast development of custom signal flows.

**Rev. PrD**


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### REVISION HISTORY

Revision Pr A1: Initial Preliminary Version

Revision Pr B1. Extra Content Added

Revision Pr B2. Added filter specs

Revision Pr B3. Added Typical Performance graphs

Revision Pr B4. Added Typical Application Circuit

# SPECIFICATIONS

**Table 1. Tests conditions unless otherwise noted.**

| | |
|---|---|
| Supply Voltage | AVDDn[2] = 3.3V, OVDD=3.3V , DVDD = Internal Voltage Regulator |
| Ambient Temperature | 25°C |
| Master Clock | TBD |
| Measurement Bandwidth | 20Hz to 20kHz |
| ADC Input Signal, DAC Output Signal | 1kHz |

**Table 2. Performance Paramters**

| Parameter | Min | Typical | Max | Units | Test Conditions/Comments |
|---|---|---|---|---|---|
| REFERENCE SECTION[1] | | | | | |
| Absolute Voltage $V_{REF}$ | | 1.5 | | V | |
| $V_{REF}$ Temperature Coefficient | | TBD | | ppm/°C | |
| AUX ANALOG INPUTS[1] (Single Ended) | | | | | |
| Number of channels | | 8 | | | 4 stereo channels |
| Full Scale Analog Input | | 100 | | uArms | 2Vrms input with 20kΩ series resistor |
| DC Offset | | 50 | | mV | Relative to $V_{REF}$ |
| ADC SECTION[1] | | | | | Stereo ADC |
| Resolution | | 24 | | Bits | |
| Dynamic Range | | | | | -60dB with respect to full scale Analog input |
| A-Weighted | | 100 | | dB | |
| Total Harmonic Distortion + Noise | | -95 | | dB | -3dB with respect to full scale Analog input |
| Interchannel Gain Mismatch | | TBD | | dB | Left and Right channel Gain Mismatch |
| Crosstalk | | TBD | | dB | Analog Channel Crosstalk (AINYm[2] to AINYm[2]) |
| Gain Error | | TBD | | dB | |
| Power Supply Rejection | | TBD | | dB | 1kHz, 300m$V_{P-P}$ Signal at AVDDn[2] |
| ADC DIGITAL DECIMATOR FILTER CHARACTERISTICS (at 48kHz) | | | | | |
| Pass Band | | 22.5 | | kHz | |
| Pass Band Ripple | | ±0.0002 | | dB | |
| Transistion Band | | 24 | | kHz | |
| Stop Band | | 26.5 | | kHz | |
| Stop Band Attenuation | | 100 | | dB | |
| Group Delay | | TBD | | µS | |
| DAC OUTPUTS [1](Single Ended) | | | | | |
| Number of channels | | 8 | | | 4 stereo output channels |
| Resolution | | 24 | | Bits | |
| Full Scale Analog Output | | 1 | | Vrms | |
| Dynamic Range | | | | | -60dB with respect to full scale code input |
| A-Weighted | | 100 | | dB | |
| Total Harmonic Distortion + Noise | | -95 | | dB | -3dB with respect to full scale code input |
| Crosstalk | | TBD | | dB | Analog Channel Crosstalk (VOUTm[2] to VOUTm[2]) |
| Gain Error | | TBD | | dB | |
| Interchannel Gain Mismatch | | TBD | | dB | Left and Right channel Gain Mismatch |
| DC Offset | | 50 | | mV | Relative to $V_{REF}$ |
| Power Supply Rejection | | TBD | | dB | 1kHz, 300m$V_{P-P}$ Signal at AVDDn[2] |
| DAC DIGITAL INTERPOLATION FILTER CHARACTERISTICS (at 48kHz) | | | | | |
| Pass Band | | 21.769 | | kHz | |
| Pass Band Ripple | | ±0.01 | | dB | |
| Transistion Band | | 23.95 | | kHz | |
| Stop Band | | 26.122 | | kHz | |
| Stop Band Attenuation | | 70 | | dB | |
| Group Delay | | 446.35 | | µS | |

| Parameter | Min | Typical | Max | Units | Test Conditions/Comments |
|---|---|---|---|---|---|
| HEADPHONE OUTPUT[1] (Single Ended) | | | | | Measured at Headphone output with 32Ω Load |
| Number of channels | | 2 | | | 1 stereo channel |
| Resolution | | 24 | | Bits | |
| Full Scale Analog Output | | 1 | | Vrms | |
| Dynamic Range | | | | | -60dBFS with respect to full scale code input |
| A-Weighted | | 95 | | dB | |
| Total Harmonic Distortion + Noise | | -75 | | dB | -3dBFS with respect to full scale code input |
| Gain Error | | TBD | | dB | |
| Interchannel Gain Mismatch | | TBD | | dB | |
| DC Offset | | 50 | | mV | Relative to $V_{REF}$ |
| Power Supply Rejection | | TBD | | dB | 1kHz, 300mV$_{P-P}$ Signal at AVDDn[2] |
| PLL SECTION[1] | | | | | |
| Master Clock Input (MCLKI) | 64x $f_S$ | | 512 x $f_S$ | MHz | |
| System Clock Output (MCLKO) | | TBD | | MHz | |
| SRC[1,3] | | | | | |
| Dynamic Range | | | | | -60 dBFS Input ( Worst case Input $f_S$ = 50kHz) |
| A-Weighted | | 115 | | dB | |
| Total Harmonic Distortion + Noise | | -113 | | dB | 0 dBFS input ( Worst case Input $f_S$ = 50kHz) |
| Sample Rate | 5 | | 50 | kHz | Bandwidth… |
| DIGITAL INPUT/OUTPUT[1] | | | | | |
| Input Voltage HI ($V_{IH}$) | 2.0 | | ODVDD | V | |
| Input Voltage LO ($V_{IL}$) | | | 0.8 | V | |
| Input Leakage ($I_{IH}$ @ $V_{IH}$ = ODVDD) | | | 10 | µA | |
| Input Leakage ($I_{IL}$ @ $V_{IL}$ = 0V) | | | 10 | µA | |
| Output Voltage HI($V_{OH}$ @ $I_{OH}$ = 0.4mA) | 2.4 | | | V | |
| Output Voltage LO ($V_{OL}$ @ $I_{OL}$ = -3.2mA) | | | 0.4 | V | |
| Input Capacitance | | 2 | | pF | |
| SUPPLIES[1] | | | | | |
| Analog Supplies AVDDn[2] | 3.15 | 3.3 | 3.45 | V | |
| Digital Supplies DVDD | 1.6 | 1.8 | 2.0 | V | |
| Interface Supply ODVDD | 3.15 | 3.3 | 3.45 | V | |
| Supply Current – Normal Mode | | | | | MCLK=12.288MHz, ADC & DACs active, Headphone |
| Analog Current (AVDD1) | | 90 | | mA | outputs active and a driving 32Ω load |
| PLL Current (AVDD2) | | TBD | | mA | |
| Digital + Interface Current | | 167 | | mA | |
| PLL Current | | 12 | | mA | |
| Power Dissapation | | 570 | | mW | |
| Supply Current – Powerdown Mode | | | | | $\overline{\text{RESET}}$ low. MCLK=3.074MHz, AINx=AGND, DAC & |
| Analog Current | | TBD | | µA | Headphone Outputs floating. |
| Digital + Interface Current | | TBD | | µA | |
| PLL Current | | TBD | | µA | |

[1] The figures quoted are target specifications and subject to change before release
[2] "n" refers to supply number, "m" refers to channel number, "Y" refers to stereo channel identifier – L, R
[3].Guaranteed by design

# DIGITAL TIMING

| Parameter | Min | Max | Unit | Comments |
|---|---|---|---|---|
| MASTER CLOCK AND RESET | | | | |
| $f_{MCLKI}$ (MCLKI Frequency) | 3.024 | 24.576 | MHz | |
| $t_{MCH}$ (MCLKI High) | TBD | | Ns | |
| $t_{MCL}$ (MCLKI Low) | TBD | | ns | |
| $t_{RLPW}$ ($\overline{RESET}$ Low Pulse Width) | 20 | | ns | |
| $I^2C$ PORT | | | | |
| $f_{SCL}$ (SCL Clock Frequency) | | 400 | kHz | |
| $t_{SCLH}$ (SCL High) | 0.6 | | µS | |
| $t_{SCLL}$ (SCL Low) | 1.3 | | µS | |
| START CONDITION | | | | |
| $t_{SCS}$ (Setup Time) | 0.6 | | µS | Relevant for Repeated Start Condition |
| $t_{SCH}$ (Hold Time) | 0.6 | | µS | After this period the 1st clock is generated |
| $t_{DS}$ (Data Setup Time) | 100 | | ns | |
| $t_{SCR}$ (SCL Rise Time) | | 300 | ns | |
| $t_{SCF}$ (SCL Fall Time) | | 300 | ns | |
| $t_{SDR}$ (SDA Rise Time) | | 300 | ns | |
| $t_{SDF}$ (SDA Fall Time) | | 300 | ns | |
| STOP CONDITION | | | | |
| $t_{SCSH}$ (Setup Time) | 0.6 | | µS | |
| SERIAL PORTS | | | | |
| SLAVE MODE | | | | |
| $t_{SBH}$ (BCLKx High) | 40 | | ns | |
| $t_{SBL}$ (BCLKx Low) | 40 | | ns | |
| $f_{SBF}$ (BCLKx Frequency) | $64 \times f_S$ | | | |
| $t_{SLS}$ (LRCLKx Setup) | 10 | | ns | To BCLK Rising Edge |
| $t_{SLH}$ (LRCLKx Hold) | 10 | | ns | From BCLK Rising Edge |
| $t_{SDS}$ (SDINx Setup) | 10 | | ns | To BCLK Rising Edge |
| $t_{SDH}$ (SDINx Hold) | 10 | | ns | From BCLK Rising Edge |
| $t_{SDD}$ (SDOx Delay) | 10 | | ns | From BCLK Falling Edge |
| MASTER MODE | | | | |
| $t_{MLD}$ (LRCLKx Delay) | | 5 | ns | From BCLK Falling Edge |
| $t_{MDD}$ (SDOx Delay) | | 10 | ns | From BCLK Falling Edge |
| $t_{MDS}$ (SDINx Setup) | 10 | | ns | From BCLK Rising Edge |
| $t_{MDH}$ (SDINx Hold) | 10 | | ns | From BCLK Rising Edge |

# ABSOLUTE MAXIMUM RATINGS

**Table 3. Absolute Maximum Ratings**

| Parameter | Rating |
|---|---|
| DVDD to DGND | 0V to 2.2V |
| ODVDD to DGND | 0V to 4.0V |
| AVDD to AGND | 0V to 4.0V |
| AGND to DGND | -0.3V to +0.3V |
| Digital Inputs | DGND – 0.3V to ODVDD + 0.3V |
| Analog Inputs | AGND – 0.3V to ADVDD + 0.3V |
| Reference Voltage | Indefinite short circuit to ground |
| Soldering (10 s) | +300°C |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

# DIGITAL TIMING DIAGRAMS

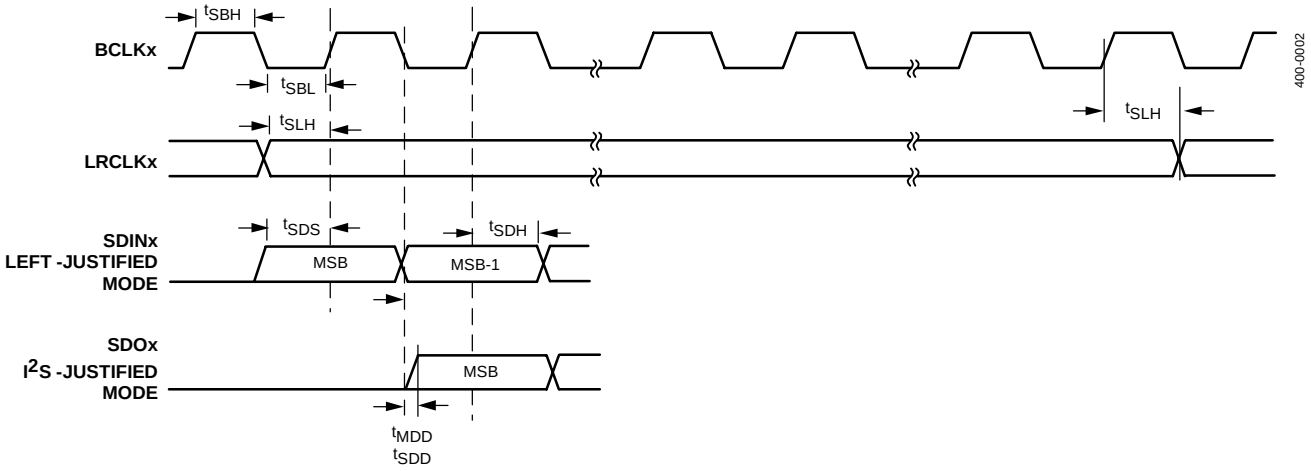


*Figure 2. Serial Port Timing*

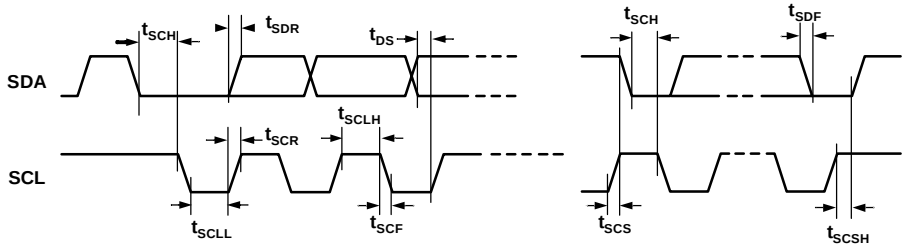


*Figure 3. I²C Port Timing*

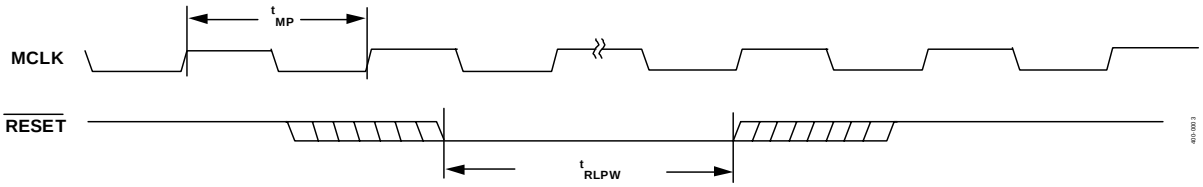


*Figure 4. Master Clock and Reset Timing*

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

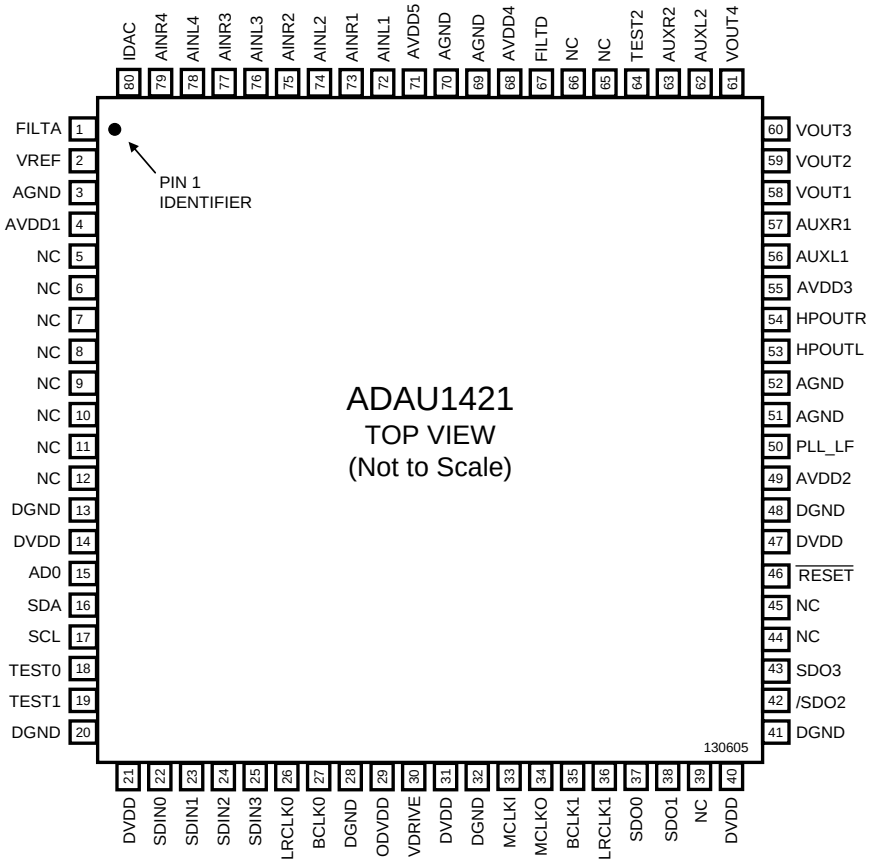


*Figure 5. 80-Lead LQFP (ST PACKAGE)*

**Table 4. Pin Function Descriptions**

| Pin No. | Name | Description |
|---|---|---|
| 1 | FILTA | ADC Filter Capacitor |
| 2 | VREF | Reference Capacitor |
| 3 | AGND | ADC Ground |
| 4 | ADVDD1 | ADC Supply (3.3V) |
| 5 | NC | Not Connected Internally |
| 6 | NC | Not Connected Internally |
| 7 | NC | Not Connected Internally |
| 8 | NC | Not Connected Internally |
| 9 | NC | Not Connected Internally |
| 10 | NC | Not Connected Internally |
| 11 | NC | Not Connected Internally |
| 12 | NC | Not Connected Internally |
| 13 | DGND | Digital Ground |
| 14 | DVDD | Digital Supply (1.8V) |
| 15 | AD0 | I2C Address – tie to ODVDD or DGND |
| 16 | SDA | I2C Data |
| 17 | SCL | I2C Clock |
| 18 | TEST0 | Test Pin. Connect to ODVDD |
| 19 | TEST1 | Test Pin. Connect to ODVDD |
| 20 | DGND | Digital Ground |
| 21 | DVDD | Digital Supply (1.8V) |
| 22 | SDIN0 | Serial Data Input 0/SRC Data Input |
| 23 | SDIN1 | Serial Data Input 1/SRC Data Input |
| 24 | SDIN2 | Serial Data Input 2/SRC Data Input |
| 25 | SDIN3 | Serial Data Input 3/SRC Data Input |
| 26 | LRCLK0 | Left-Right Clock for SRC |
| 27 | BCLK0 | Bit Clock for SRC |
| 28 | DGND | Digital Ground |
| 29 | ODVDD | Digital Interface Supply (3.3V) |
| 30 | VDRIVE | Drive for External PNP Transistor |
| 31 | DVDD | Digital Supply (1.8V) |
| 32 | DGND | Digital Ground |
| 33 | MCLKI | Master Clock Input |
| 34 | MCLKO | Audio Clock Output |
| 35 | BCLK1 | Bit Clock for Serial Data Input/Output |
| 36 | LRCLK1 | Left-Right Clock for Serial Data Input/Output |

| Pin No. | Name | Description |
|---|---|---|
| 37 | SDO0 | Serial Data Output 0 |
| 38 | SDO1 | Serial Data Output 1 |
| 39 | NC | Not Connected Internally |
| 40 | DVDD | Digital Supply (1.8V) |
| 41 | DGND | Digital Ground |
| 42 | SDO2 | Serial Data Output 2 |
| 43 | SDO3 | Serial Data Ouput 3 |
| 44 | NC | Not Connected Internally |
| 45 | NC | Not Connected Internally |
| 46 | $\overline{\text{RESET}}$ | Active Low Reset |
| 47 | DVDD | Digital Supply (1.8V) |
| 48 | DGND | Digital Ground |
| 49 | AVDD2 | PLL Supply (3.3V) |
| 50 | PLL_LF | PLL Loop Filter |
| 51 | AGND | PLL Ground |
| 52 | AGND | Headphone Driver Ground |
| 53 | HPOUTL | Left Headphone Output |
| 54 | HPOUTR | Right Headphone Output |
| 55 | AVDD3 | Headphone Driver Supply (3.3V) |
| 56 | AUXL1 | Auxiliary DAC Output Left 1 |
| 57 | AUXR1 | Auxiliary DAC Output Right 1 |
| 58 | VOUT1 | Main DAC Output 1 |

| Pin No. | Name | Description |
|---|---|---|
| 59 | VOUT2 | Main DAC Output 2 |
| 60 | VOUT3 | Main DAC Output 3 |
| 61 | VOUT4 | Main DAC Output 4 |
| 62 | AUXL2 | Auxiliary DAC Output Left 2 |
| 63 | AUXR2 | Auxiliary DAC Output Right 2 |
| 64 | NC | Not Connected Internally |
| 65 | NC | Not Connected Internally |
| 66 | NC | Not Connected Internally |
| 67 | FILTD | DAC Filter Capacitor |
| 68 | AVDD4 | DAC Supply (3.3V) |
| 69 | AGND | DAC Ground |
| 70 | AGND | DAC Ground |
| 71 | AVDD5 | DAC Supply (3.3V) |
| 72 | AINL1 | Left Analog Input 1 |
| 73 | AINR1 | Right Analog Input 1 |
| 74 | AINL2 | Left Analog Input 2 |
| 75 | AINR2 | Right Analog Input 2 |
| 76 | AINL3 | Left Analog Input 3 |
| 77 | AINR3 | Right Analog Input 3 |
| 78 | AINL4 | Left Analog Input 4 |
| 79 | AINR4 | Right Analog Input 4 |
| 80 | IDAC | DAC External Bias Resistor. Use 20kΩ to AGND |

## PIN FUNCTIONS

Table 4 shows the ADAU1421's pin numbers, names, and functions. Input pins have a logic threshold compatible with 3.3V input levels.

### *SDIN0, SDIN1, SDIN2, SDIN3*

Serial Data Inputs. These input pins provide the digital audio data to the signal processing core. Any one of the four inputs can be routed to the SRC for sample rate conversion, however this input will not then be available to the core directly but only as the output of the SRC. The serial format is selected by writing to Bits 2:0 of the Input Sport Control register. The input serial port is always a synchronous slave device. The serial port uses BCLK1 and LRCLK1 from the Output Serial Port as timing signals for SDIN0 to SDIN3.

### *LRCLK0, BCLK0*

Left/Right and Bit Clocks for the SRC. These input clocks are associated with the SDIN0 to SDIN3 signals when one of these channels is connected to the SRC.

### *SDO0, SDO1, SDO2, SDO3*

Serial Data/TDM/Data Outputs. These pins are used for serial digital outputs. For non-TDM systems, these pins can output 4 channels of digital audio, using a variety of standard two-channel formats. The configuration of the output port is set by the Output Sport Control register.

### *LRCLK1, BCLK1*

This clock pair is used as clock and frame sync signals for the SDINx and SDOx pins. These clocks are inputs to the ADAU1421 when the port is configured as a slave and outputs when the port is configured as a master. On power-up, these pins are set to slave mode to avoid conflicts with external master-mode devices.

### *MCLKI*

Master Clock Input. The ADAU1421 uses a PLL to generate the appropriate internal clock for the DSP core.

### *MCLK0*

The MCLKO pin can be programmed to output some of the internal clocks. These clocks can be used elsewhere in the system if it is required to synchronize additional components with the ADAU1421. Bits 5 to 3 in the User Control Register 1 are used to select which clock is output on this pin.

### *SDA*

Serial Data Input for the $I^2C$Control Port.

### *SCL*

Serial Clock for the $I^2C$ Control Port.

### *AD0*

Address Select. This pin selects the address for the ADAU1421's communication with the control port. This allows two ADAU1421s to be used with a single $I^2C$ port.

**$\overline{\text{RESET}}$**

Active-Low Reset Signal. After $\overline{\text{RESET}}$ goes high, all the circuit blocks of the ADAU1421 are powered down. The blocks can be individually powered up by programming the appropriate bits in the Power Control register. When the audio processor core is powered up it takes 3072 MCLK cycles to initialize the internal circuitry. The user should not attempt to load a new program during this period. When the core is powered up it takes approximately 32768 MCLK periods to initialize the data RAM. The data RAM will not be available during this time.

***AINL1, AINL2, AINL3, AINL4***
***AINR1, AINR2, AINR3, AINR4***

Analog inputs which are connected via a multiplexer to the on-chip ADC. The analog inputs are current inputs and should be driven via a 20kΩ resistor as shown in Figure 16.

***VOUT1, VOUT2, VOUT3, VOUT4***

Analog outputs from the on-chip DAC.

***AUXL1, AUXR1, AUXL2, AUXR2***

Analog outputs from the on-chip auxiliary DACs.

***HPOUTL, HPOUTR***

Analog outputs from the headphone amplifiers.

***PLL_LF***

PLL Loop filter connection. External components are required to allow the PLL to function correctly. See the PLL section for details of these components.

***VREF***

Voltage Reference for Regulator. This pin is driven by an internal 1.5V reference voltage.

***FILTA, FILTD***

Decoupling nodes for the ADC and DAC respectively. Decoupling capacitors should be connected between these nodes and AGND.

***VDRIVE***

Drive for External Transistor. The base of the voltage regulator's external PNP transistor is driven from this pin.

***AVDD1, AVDD2, AVDD3, AVDD4, AVDD5***

Analog power supply pins. These pins should be connected to +3.3V. Each pin should be decoupled with a 10µF and 0.1µF capacitor to AGND as close to the pin as possible.

***DVDD (4)***

Digital power supply pins. These pins should be connected to +1.8V, either directly or by using the on-chip regulator. Each pin should be decoupled with a 10µF and 0.1µF capacitor to DGND as close to the pin as possible.

***ODVDD***

Digital interface power supply pin. This pin should be connected to a +3.3V digital supply. The pin should be decoupled with a 10µF and 0.1µF capacitor to ADGND as close to the pin as possible.

***DGND***

Digital ground.

***AGND***

Analog ground.

***IDAC***

This is an external bias pin for the DAC circuitry. A 20kΩ resistor should be connected between this pin and AGND.

# TYPICAL PERFORMANCE CHARACTERISTICS

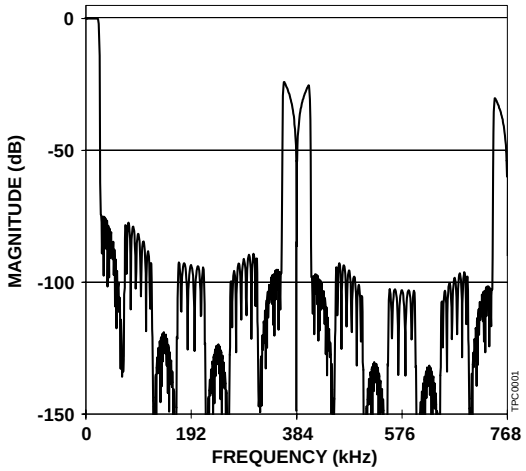


*Figure 6. DAC Composite Filter Response (48kHz)*

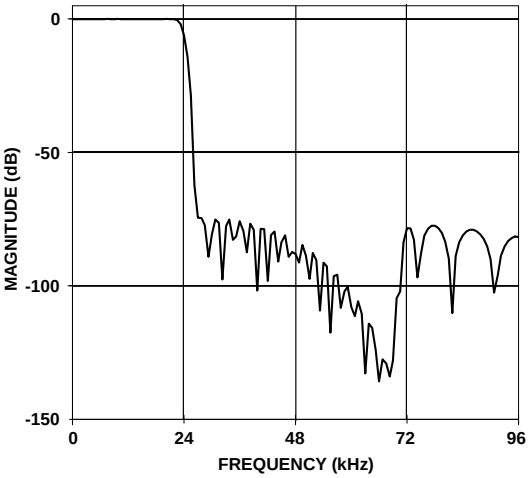


*Figure 7. DAC Pass Band Filter Response (48kHz)*

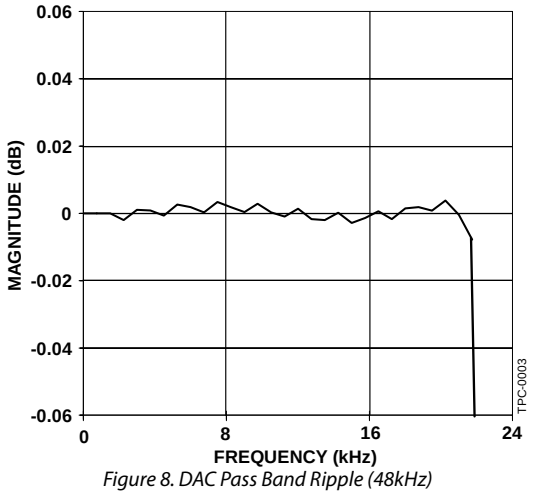


*Figure 8. DAC Pass Band Ripple (48kHz)*

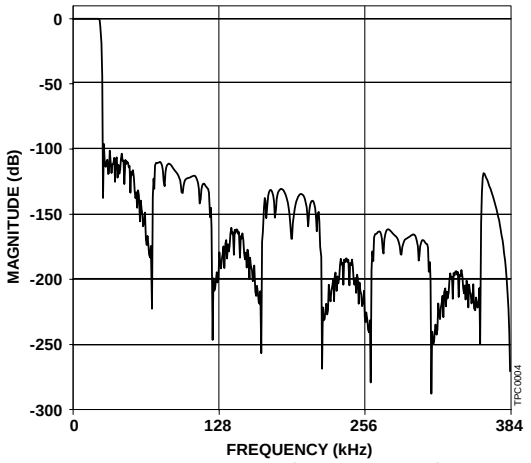


*Figure 9. ADC Composite Filter Response (48kHz)*

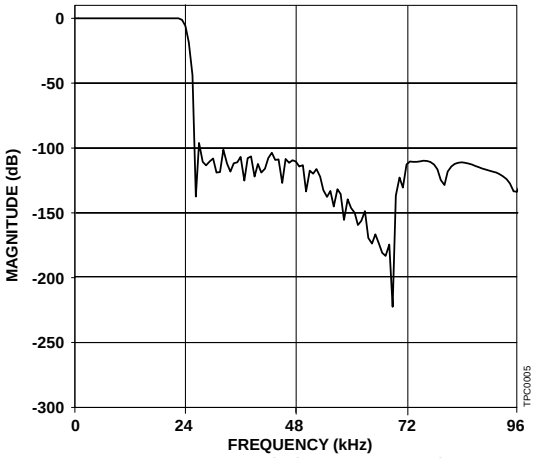


*Figure 10. ADC Pass Band Filter Response (48kHz)*

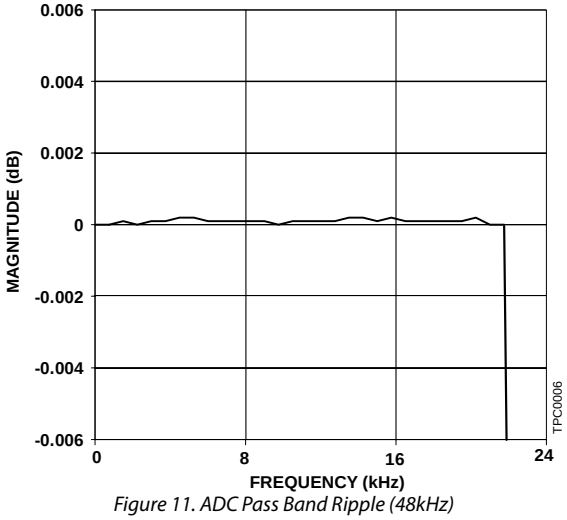


*Figure 11. ADC Pass Band Ripple (48kHz)*

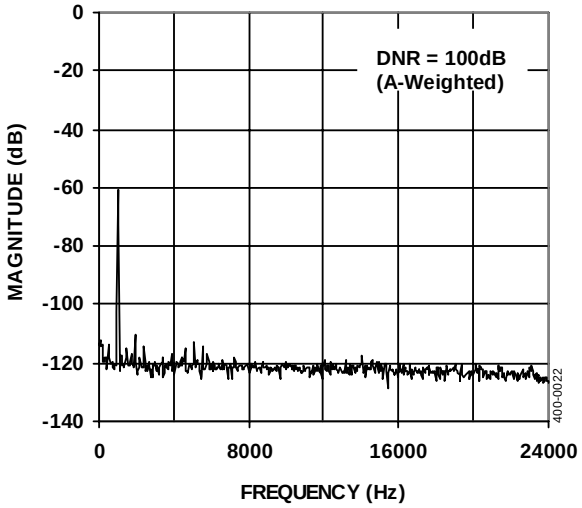


*Figure 12. DAC Dynamic Range*

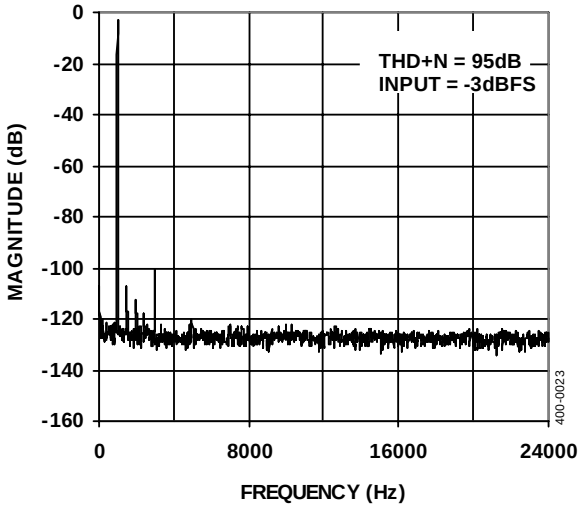


*Figure 13. DAC Total Harmonic Distortion plus Noise*

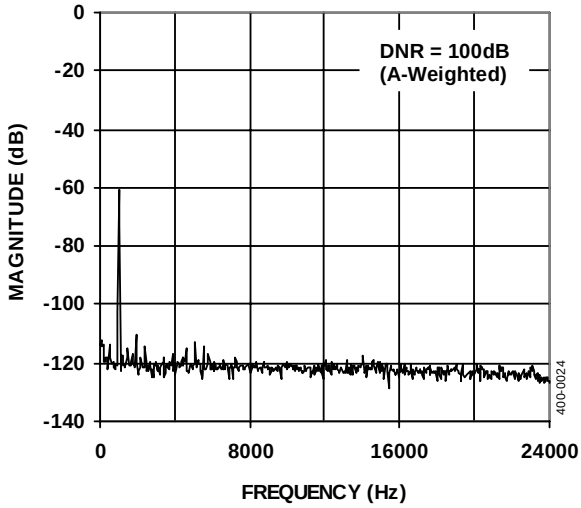


*Figure 14. ADC Dynamic Range*

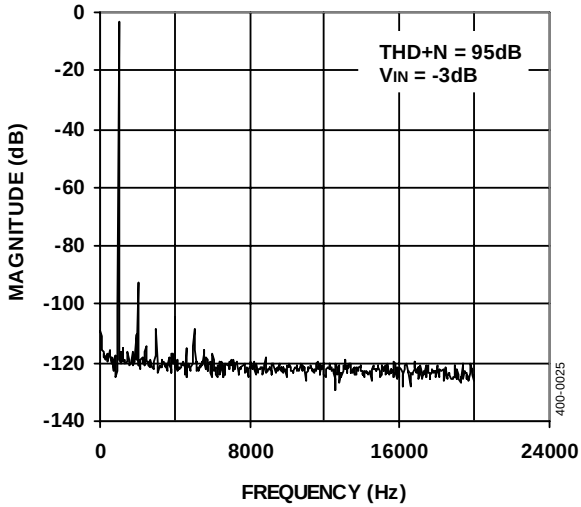


*Figure 15. ADC Total Harmonic Distortion plus Noise*

# FEATURES

The ADAU1421 is an enhanced audio processor. It contains a digital processing core based on ADI's SigmaDSP™ technology. The digital processor accepts digital inputs from up to 4 stereo channels, typically operating at 48 kHz. A sample rate converter (SRC) is included allowing a single stereo channel be converted from a different rate to 48 kHz to allow it to be processed. In addition any of four stereo analog sources can be processed by converting them to digital data via the high performance on-chip ADC. Processed data is available in digital form as a standard audio stream such as. The processed audio data can also be converted to analog form by using the four high performance on-chip stereo DACs.

The core of the ADAU1421 is a 28-bit DSP (56-bit with double precision) optimized for audio processing. Signal processing parameters are stored in a 1024-location parameter RAM and the program RAM can be loaded with a custom program after power-up. New values are written to the program and parameter RAM using the control port. The values stored in the parameter RAM control individual signal processing blocks, such as IIR equalization filters, dynamics processors, audio delays, and mixer levels. A safeload feature allows parameters to be transparently updated without causing clicks on the output signals.

The target/slew RAM contains 64 locations and can be used as channel volume controls or for other parameter updates. These RAM locations take a target value for a given parameter and ramp the current parameter value to the new value using a specified time constant and one of a selection of linear or logarithmic curves.

The ADAU1421 has a sophisticated control port that supports complete read/write capability of all memory locations.

The ADAU1421 has very flexible serial data input/output ports that allows for glueless interconnection to a variety of ADCs, DACs, general-purpose DSPs, S/PDIF receivers, and sample rate converters. The digital inputs and outputs of the ADAU1421 can be configured in I²S, left-justified or right-justified, or TDM serial port compatible modes. It can support 16, 20, and 24 bits in all modes. The ADAU1421 accepts serial audio data in MSB first and twos complement format.

The digital core of ADAU1421 operates at 1.8V and the other circuit blocks operate from a 3.3V power supply. An on-board regulator allows a single 3.3V supply be used for both digital supplies using the configuration shown in Figure 19.
The ADAU1421 is fabricated on a single monolithic integrated circuit and is housed in a 80-lead LQFP package for operation over the -40°C to +105°C automotivel temperature range.

## ANALOG INPUT MULTIPLEXER

ADAU1421 has eight analog input channels arranged as 4 stereo pairs. Any one of these stereo channels can be connected to a high performance ADC. The digital output of the ADC can then be used by the audio processor core. The ADC multiplexer is controlled by bits 3 to 0 of the ADC Input MUX Register. Only one of these bits should be set at a time. The ADC, ADC Digital Engine and Reference Buffer need to be powered up if the ADC is to be used. This can be achieved by setting bits 14, 13 and 1 of the Power Control Register. The analog input is a current input by default but can be converted to a voltage input by using series resistors as shown in Figure 16.

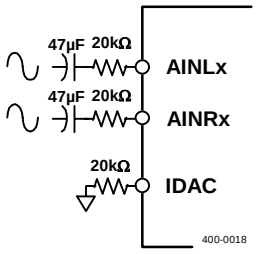


*Figure 16. Analog Input Configuration*

## SAMPLE RATE CONVERTER BLOCK

The ADAU1421 contains a Sample Rate Converter (SRC) to allow input sample rates other 48 kHz be used as a digital input. The SRC is powered up by setting the SRC bit in the Power Control Register. To use the SRC the user programs bits 6 and 5 in the SRC Serial Port Control Register to select which one of the four SDIN channels is connected to the input of the SRC. Since using the SRC implies that one of the SDIN inputs is at a sample rate other than the default 48kHz it should not be used by the audio processor core. To prevent this input from being available to the core the SRC Mux Enable bit should be set. This bit enables the SRC input multiplexer and also masks the selected input so that is not available to the audio processor core. When the SRC Mux Enable bitis 0 SDIN3 appears at the output of the SRC. Figure 17 shows how the SRC block is configured. Note that the SRC has a filter cutoff frequency of 20kHz for a 48kHz sample rate. If a different sample rate is used the cutoff frequency scales accordingly.

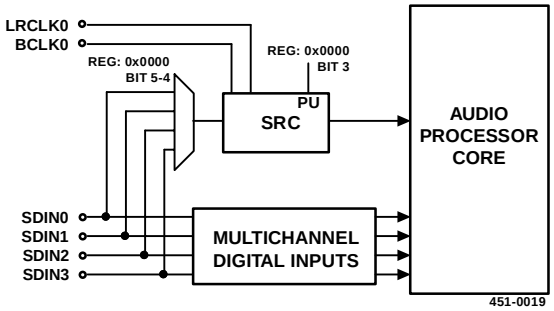


*Figure 17. SRC Input Configuration*

## PLL BLOCK

The ADAU1421 contains a PLL which generates all the clocks required by the system from a single input source. An input clock source is required. The clock frequency can be 64 × $f_S$, 128 × $f_S$, 256 × $f_S$, or 512 × $f_S$. Bits 2 and 1 in the User Control Register 1 should be programmed for the appropriate clock frequency to ensure that the correct clock frequencies are generated. The PLL is powered down by default and Bit 15 the Power Control Register must be set to use the PLL. Bit 0 of User Control Register 1 determines whether the PLL is used or not. After a reset this bit is cleared indicating that the PLL is not used and the clock on the MCLKI pin is used by the audio processing core. This will allow the user to write to the part while the PLL is off. The user should power up the PLL and set bit 0 of User Control Register 1 to enable the PLL so it can generate all the clocks required for normal operation.

The PLL requires some external components to operate correctly. These components, shown in Figure 18 form a loop filter which integrates the current pulses from a charge pump and produces a voltage which is used to tune the VCO. Good quality capacitors, such as PPS film, are recommended.

A 3.3V analog supply is required to operate the PLL. Where the supply for AVDD1 is also to be used for the SRC additional filtering is recommend to prevent digital noise created by the PLL block being coupled to the analog circuitry powered by the AVDD1 supply.

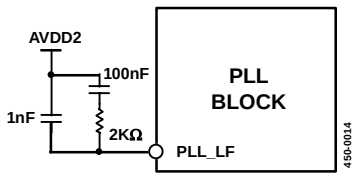


*Figure 18. PLL Loop Filter Components*

## ANALOG OUTPUTS

The ADAU1421 contains eight high performance DACs arranged as 4 stereo pairs. The DACs are the main outputs from the audio processor core. One pair of DACs are connected to integrated headphone amplifiers although the outputs are also available on the AUXL1 and AUXR1 pins. Each stereo DAC has independent power control and are powered down by default. The DACs can be powered up by setting the appropriate bit in the Power Control Register.

## VOLTAGE REGULATOR

The ADAU1421 includes an on-chip voltage regulator that allows the chip to be used in systems where a 1.8 V supply is not available, but 3.3 V is. The only external components needed for this are a PNP transistor such as an FZT953, a single capacitor, and a single resistor. The recommended design for the voltage regulator is shown in Figure 19. The 10 µF capacitor shown in this schematic is recommended for bypassing, but is not necessary for operation. Here, VDD is the main system voltage (3.3 V) and should be connected to VSUPPLY. 1.8 V is generated at the transistor's collector, which is connected to the DVDD pins. The reference voltage on VREF is 1.15 V and is generated by the regulator. VDRIVE is connected to the base of the PNP transistor and a 1 kΩ resistor should be connected between VDRIVE and VDD.

If the regulator is not used in the design, VDRIVE should be tied to ground.

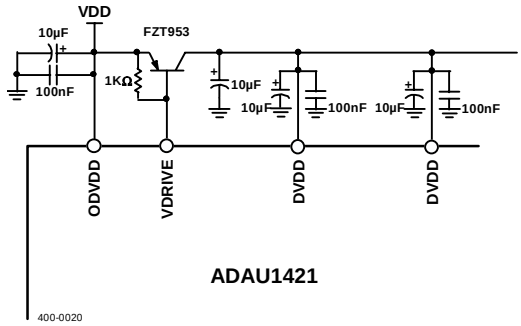


*Figure 19. Voltage Regulator Design*

# SIGNAL PROCESSING

The ADAU1421 is designed to provide all signal processing functions commonly used in stereo or multi-channel playback systems. The signal processing flow is set by using the ADI-supplied software, which allows graphical entry and real-time control of all signal processing functions.

Many of the signal processing functions are coded using full, 56-bit double-precision arithmetic. The input and output word lengths are 24 bits. Four extra headroom bits are used in the processor to allow internal gains up to 24 dB without clipping. Additional gains can be achieved by initially scaling down the input signal in the signal flow.

The signal processing blocks can be arranged in a custom program that can be loaded to the ADAU1421's RAM. The available signal processing blocks are explained in the following sections.

## NUMERIC FORMATS

It is common in DSP systems to use a standardized method of specifying numeric formats. Fractional number systems are specified by an A.B format, where A is the number of bits to the left of the decimal point and B is the number of bits to the right of the decimal point.

The ADAU1421 use the same numeric format for both the coefficient values (stored in the parameter RAM) and the signal data values. The format is as follows:

### *Numerical Format: 5.23*

Range: –16.0 to (+16.0 – 1 LSB)

Examples:
1000 0000 0000 0000 0000 0000 0000 = –16.0
1110 0000 0000 0000 0000 0000 0000 = –4.0
1111 1000 0000 0000 0000 0000 0000 = –1.0
1111 1110 0000 0000 0000 0000 0000 = –0.25
1111 1111 1111 1111 1111 1111 1111 = (1 LSB below 0.0)
0000 0000 0000 0000 0000 0000 0000 = 0.0
0000 0010 0000 0000 0000 0000 0000 = 0.25
0000 1000 0000 0000 0000 0000 0000 = 1.0
0010 0000 0000 0000 0000 0000 0000 = 4.0
0111 1111 1111 1111 1111 1111 1111 = (16.0 – 1 LSB).

The serial port accepts up to 24 bits on the input and is sign-extended to the full 28 bits of the core. This allows internal gains of up to 24 dB without encountering internal clipping.

A digital clipper circuit is used between the output of the DSP core and the serial output ports (see Figure 20). This clips the top four bits of the signal to produce a 24-bit output with a range of 1.0 (minus 1 LSB) to –1.0.

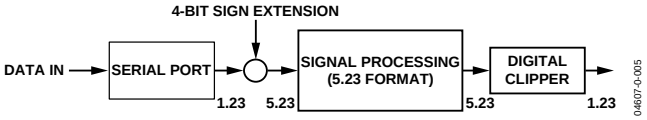


*Figure 20. Numeric Precision and Clipping Structure*

## PROGRAMMING

On power-up, the ADAU1421's default program passes the unprocessed input signals to the outputs but the outputs are muted by default. There are 2560 instruction cycles per audio sample. This DSP runs in a stream-oriented manner, meaning all 2560 instructions are executed each sample period. The ADAU1421 may also be set up to accept double- or quad-speed inputs by reducing the number of instructions/sample, which can be set in the core control register.

The part can be easily programmed using graphical tools provided by Analog Devices. No knowledge of writing DSP code is needed to program the ADAU1421. The user can simply connect graphical blocks such as biquad filters, dynamics processors, mixers, and delays in a signal flow schematic. The schematic is then compiled and the program and parameter files loaded into the ADAU1421's program RAM through the control port. Signal processing blocks available in the provided libraries include

- Single and double precision bi-quad filters
- Mono and multi-channel dynamics processors
- Mixers and splitters
- Tone and noise generators
- First-order filters
- Fixed and variable gain
- RMS look-up tables
- Loudness
- Delay
- Stereo enhancement (Phat Stereo™)
- Dynamic bass boost
- Interpolators and decimators

Additional blocks are always in development. Analog Devices also provides proprietary and third-party algorithms for applications such as matrix decoding, bass enhancement, and surround virtualizers. Please contact ADI for information about licensing these algorithms.

# CONTROL PORT

## OVERVIEW

The ADAU1421 has many different control options that can be set through an I²C interface. The ADAU1421 uses a 2-wire I²C bus control port. Most signal processing parameters are controlled by writing new values to the parameter RAM using the control port. Other functions, such as mute and input/output mode control, are programmed by writing to the control registers.

The control port is capable of full read/write operation for all of the memories and registers. All addresses may be accessed in either single-address mode or burst mode. A control word consists of the chip address, the register/RAM subaddress, and the data to be written. The number of bytes per word depends on the type of data that is being written.

The first byte of a control word (Byte 0) contains the 7-bit chip address plus the R/$\overline{W}$ bit. The next two bytes (Bytes 1 and 2) together form the subaddress of the memory or register location within the ADAU1421. This subaddress needs to be two bytes because the memories within the ADAU1421 are directly addressable, and their sizes exceed the range of single-byte addressing. All subsequent bytes (Bytes 3, 4, etc.) contain the data, such as control port data or program or parameter data.

The exact formats for specific types of writes are shown in Table 17 to Table 26.

The ADAU1421 have several mechanisms for updating signal processing parameters in real time without causing pops or clicks. In cases where large blocks of data need to be down-loaded, the output of the DSP core can be halted (using Bit 9 of the core control register), new data loaded, and then restarted. This is typically done during the booting sequence at start-up or when loading a new program into RAM. In cases where only a few parameters need to be changed, they can be loaded without halting the program. To avoid unwanted side effects while loading parameters on the fly, the SigmaDSP provides the safeload registers. The safeload registers can be used to buffer a full set of parameters (e.g. the five coefficients of a biquad) and then transfer these parameters into the active program within one audio frame. The safeload mode uses internal logic to prevent contention between the DSP core and the control port.

## ADAU1421 I²C PORT

The ADAU1421 supports a 2-wire serial (I²C-compatible) micro-processor bus driving multiple peripherals. Two pins, serial data (SDA) and serial clock (SCL), carry information between the ADAU1421 and the system I²C master controller. The ADAU1421 is always a slave on the I²C bus, which means that it never initiates a data transfer. Each slave device is recognized by a unique address. The ADAU1421 has four possible slave addresses, two for writing operations and two for reading. These are unique addresses for the device and are illustrated in Table 5. The LSB of the byte sets either a read or write operation; Logic Level 1 corresponds to a read operation and Logic Level 0 corresponds to a write operation. The seventh bit of the address is set by tying the AD0 pin of the ADAU1421 to Logic Level 0 or Logic Level 1.

**Table 5. ADAU1421 I²C Addresses**

| AD0 | R/$\overline{W}$ | Slave Address |
|---|---|---|
| 0 | 0 | 0x28 |
| 0 | 1 | 0x29 |
| 1 | 0 | 0x2A |
| 1 | 1 | 0x2B |

### *Addressing*

Initially, all devices on the I²C bus are in an idle state, which is where the devices monitor the SDA and SCL lines for a start condition and the proper address. The I²C master initiates a data transfer by establishing a Start condition, defined by a high-to-low transition on SDA while SCL remains high. This indicates that an address/data stream will follow. All devices on the bus respond to the start condition and read the next byte (7-bit address + R/$\overline{W}$ bit) MSB-first. The device that recognizes the transmitted address responds by pulling the data line low during the ninth clock pulse. This ninth bit is known as an acknowledge bit. All other devices withdraw from the bus at this point and return to the idle condition. The R/W bit determines the direction of the data. A Logic 0 on the LSB of the first byte means the master will write information to the peripheral. A Logic 1 on the LSB of the first byte means the master will read information from the peripheral. A data transfer takes place until a stop condition is encountered. A stop condition occurs when SDA transitions from low to high while SCL is held high. Figure 21 shows the timing of an I²C write.

Burst mode addressing, where the subaddresses are automatically incremented at word boundaries, can be used for writing large amounts of data to contiguous memory locations. This increment happens automatically if a stop condition is not encountered after a single-word write. The registers and memories in the ADAU1421 range in width from one to six bytes, so the auto-increment feature knows the mapping between sub-addresses and the word length of the destination register (or memory location). A data transfer is always terminated by a stop condition.

Stop and start conditions can be detected at any stage during the data transfer. If these conditions are asserted out of sequence with normal read and write operations, these cause an immediate jump to the idle condition. During a given SCL high period, the user should only issue one start condition, one stop condition, or a single stop condition followed by a single start condition. If an invalid subaddress is issued by the user, the

ADAU1421 does not issue an acknowledge and returns to the idle condition. If the user exceeds the highest subaddress while in auto-increment mode, one of two actions will be taken. In read mode, the ADAU1421 outputs the highest subaddress register contents until the master device issues a no-acknowledge, indicating the end of a read. A no-acknowledge condition is where the SDA line is not pulled low on the ninth clock pulse on SCL.

### *I²C Read and Write Operations*

Table 6 shows the timing of a single-word write operation. Every ninth clock, the ADAU1421 issues an acknowledge by pulling SDA low.

Table 7 shows the timing of a burst mode write sequence. This figure shows an example where the target destination registers are two bytes. The ADAU1421 knows to increment its subaddress register every two bytes because the requested subaddress corresponds to a register or memory area with a 2-byte word length.

The timing of a single word read operation is shown in Table 8. Note that the first R/$\overline{W}$ bit is still a 0, indicating a write operation. This is because the subaddress still needs to be written in order to set up the internal address. After the ADAU1421 acknowledges the receipt of the subaddress, the master must issue a repeated start command followed by the chip address byte with the R/$\overline{W}$ set to 1 (read). This causes the ADAU1421's SDA to turn around and begin driving data back to the master. The master then responds every ninth pulse with an acknow-ledge pulse to the ADAU1421.

Table 9 shows the timing of a burst-mode read sequence. This figure shows an example where the target read registers are two bytes. The ADAU1421 knows to increment its subaddress register every two bytes because the requested subaddress corresponds to a register or memory area with word lengths of two bytes. Other address ranges may have a variety of word lengths ranging from one to six bytes; the ADAU1421 always decodes the subaddress and sets the autoincrement circuit so that the address increments after the appropriate number of bytes.

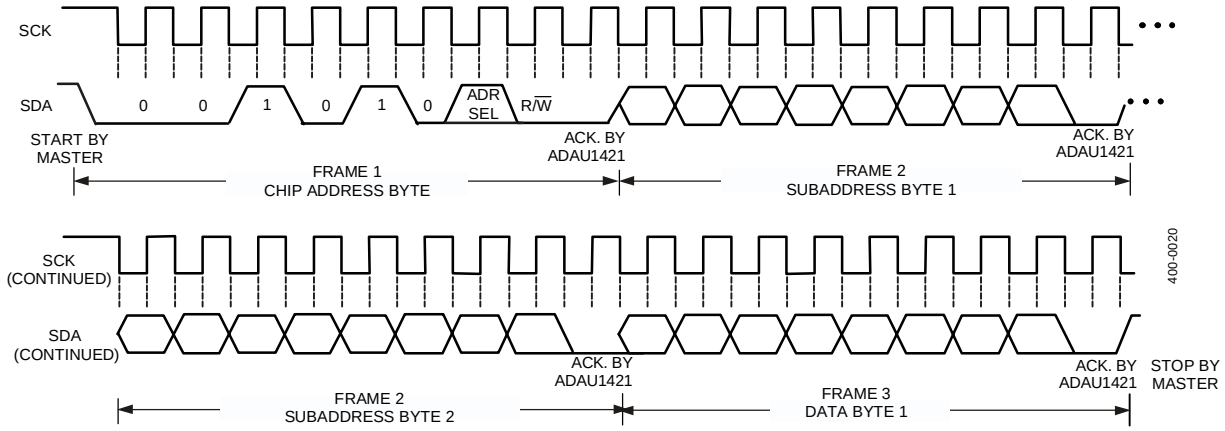


*Figure 21. ADAU1421 I²C Write Format*

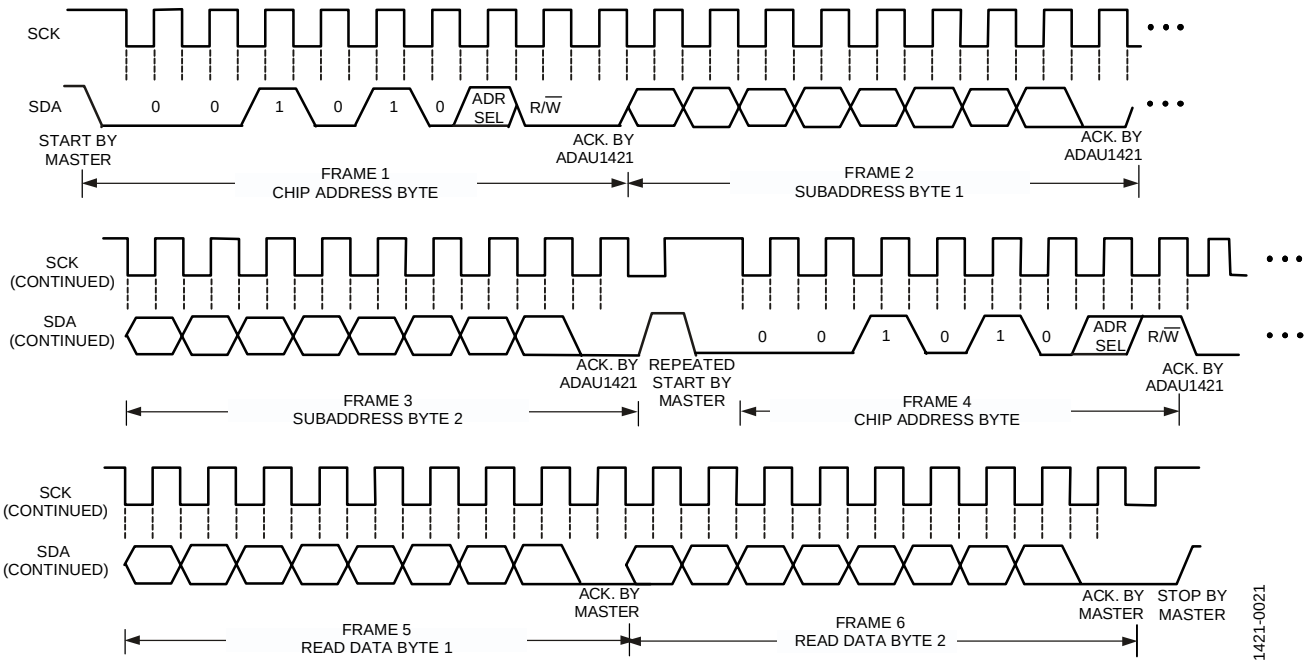


*Figure 22. ADAU1421 I²C Read Format*

**Table 6. Single-Word I²C Write**

| S | Chip Address, R/W=0 | AS | Subaddress High | AS | Subaddress Low | AS | Data Byte 1 | AS | Data Byte 2 | … | AS | Data Byte N | P |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

**Table 7. Burst Mode I²C Write**

| S | Chip Address, R/W=0 | AS | Subaddress High | AS | Subaddress Low | AS | Data Word 1 Byte 1 | AS | Data Word 1 Byte 2 | AS | Data Word 2 Byte 1 | AS | Data Word 2 Byte 2 | AS | … | P |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

**Table 8. Single Word I²C Read**

| S | Chip Address, R/W=0 | AS | Subaddress High | AS | Subaddress Low | AS | S | Chip Address R/W=1 | AS | Data Byte 1 | AM | Data Byte 2 | … | AM | Data Byte N | P |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

**Table 9. Burst Mode I²C Read**

| S | Chip Address, R/W=0 | AS | Subaddress High | AS | Subaddress Low | AS | S | Chip Address R/W=1 | AS | Data Word 1 Byte 1 | AM | Data Word 1 Byte 2 | AM | … | P |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

S - Start Bit
P - Stop Bit
AM - Acknowledge by Master
AS - Acknowledge by Slave

# RAMS AND REGISTERS

**Table 10. Control Port Addresses**

| I²C Subaddress | Register Name | Read/Write Word Length |
|---|---|---|
| 0–1023 (0x0000–0x03FF) | Parameter RAM | Write: 4 Bytes, Read: 4 Bytes |
| 1024–4095 (0x0400–0x0FFF) | Program RAM | Write: 6 Bytes, Read: 6 Bytes |
| 4096–4159 (0x1000–0x103F) | Target/Slew RAM | Write: 5 Bytes, Read: N/A |
| 4160–4164 (0x1040–0x1044) | Parameter RAM Data Safeload Registers 0–4 | Write: 5 Bytes, Read: N/A |
| 4165–4169 (0x1045–0x1049) | Parameter RAM Indirect Address Safeload Registers 0-4 | Write: 2 Bytes, Read: N/A |
| 4170–4175 (0x104A–0x104F) | Data Capture Registers 0–5 (Control Port Readback) | Write: 2 Bytes, Read: 3 Bytes |
| 4176–4177 (0x1050–0x1051) | Data Capture Registers (Digital Output) | Write: 2 Bytes, Read: N/A |
| 4178 (0x1052) | Audio Core Control Register | Write: 2 Bytes, Read: 2 Bytes |
| 4179 (0x1053) | RAM Modulo Control Register | Write: 1 Byte, Read: 1 Byte |
| 4180 (0x1054) | Serial Output Control Register | Write: 2 Bytes, Read: 2 Bytes |
| 4181 (0x1055) | Serial Input Control Register | Write: 1 Byte, Read: 1 Byte |
| 4182 (0x1056) | SRC Serial Port Control Register | Write: 1 Byte, Read: 1 Byte |
| 4183 (0x1057) | ADC Input Mux Control Register | Write: 2 Bytes, Read: 2 Bytes |
| 4184 (0x1058) | Power Control Register | Write: 2 Bytes, Read: 2 Bytes |
| 4185 (0x1059) | User Control 1 Register | Write: 2 Bytes, Read: 2 Bytes |
| 4186 (0x105A) | User Control 2 Register | Write: 2 Bytes, Read: 2 Bytes |

**Table 11. RAM Read/Write Modes**

| Memory | Size | Subaddress Range | Read | Write | Burst Mode Available | Write Modes |
|---|---|---|---|---|---|---|
| Parameter RAM | 1024 × 28 | 0–1023 (0x0000–0x03FF) | Yes | Yes | Yes | Direct Write[1] Safeload Write |
| Program RAM | 3072 × 42 | 1024–4095 (0x0400–0x0FFF) | Yes | Yes | Yes | Direct Write[1] |
| Target/Slew RAM | 64 × 34 | 4096–4159 (0x1000–0x1044) | No | Yes | Yes[2] | Direct Write[3] Safeload Write |

[1] DSP core should be shut down first to avoid clicks/pops.
[2] The target/slew RAMs need to be written through the safeload registers. Safeload writes may be done in either single-write or burst-mode.
[3] DSP core should be shut down first to avoid clicks/pops.

## CONTROL PORT ADDRESSING

Table 10 shows the addressing of the ADAU1421's RAM and register spaces. The address space encompasses a set of registers and three RAMs: one each for holding signal processing parameters, holding the program instructions, and ramping parameter values. The program and parameter RAMs are initialized on power-up. Table 11 shows the sizes and available writing modes of the parameter, program, and target/slew RAMs.

## PARAMETER RAM CONTENTS

The parameter RAM is 28 bits wide and occupies Addresses 0 to 1023. The parameter RAM is initialized to all 0s on power-up. The data format of the parameter RAM is twos complement 5.23. This means that the coefficients may range from +16.0 (minus 1 LSB) to –16.0, with 1.0 represented by the binary word 0000 1000 0000 0000 0000 0000 0000.

### *Options for Parameter Updates*

The parameter RAM can be written and read using one of the two following methods.

1. **Direct Read/Write**. This method allows direct access to the program and parameter RAMs. This mode of operation is normally used during a complete new load of the RAMs, using burst-mode addressing. The clear registers bit in the core control register should be set to 0 using this mode to avoid any clicks or pops in the outputs. Note that it is also possible to use this mode during live program execution, but since there is no handshaking between the core and the control port, the parameter RAM will be unavailable to the DSP core during control writes, resulting in clicks and pops in the audio stream.

2. **Safeload Write.** Up to five safeload registers can be loaded with parameter RAM address/data. The data is then transferred to the requested address when the RAM is not busy. This method can be used for dynamic updates while live

program material is playing through the ADAU1421. For example, a complete update of one biquad section can occur in one audio frame, while the RAM is not busy. This method is not available for writing to the program RAM or control registers. The following sections discuss these two options in more detail.

## RECOMMENDED PROGRAM/PARAMETER LOADING PROCEDURES

When writing large amounts of data to the program or parameter RAM in direct write mode, the processor core should be disabled to prevent unpleasant noises from appearing at the audio output. The ADAU1421 contain several mechanisms for disabling the core.

If the loaded program does NOT use the target/slew RAM as the main system volume control (for example, the default power-up program)

1. Assert Bit 9 (LOW to assert—default setting) and Bit 6 (HIGH to assert) of the core control register. This zeroes the accumulators, the serial output registers, and the serial input registers.
2. Fill the program RAM using burst mode writes.
3. Fill the parameter RAM using burst mode writes.
4. Assert Bit 7 of the core control register to initiate a data-memory clear sequence. Wait at least 100 µs for this sequence to complete. This bit is automatically cleared after the operation is complete.
5. Deassert Bit 9 and Bit 6 of the core control register to allow the core to begin normal operation

If the loaded program does use the target/slew RAM as the main system volume control:

1. Assert Bit 12 of the core control register. This begins a volume ramp-down, with a time constant determined by the upper bits of the target RAM. Wait for this ramp-down to complete (the user may poll Bit 13 of the core control register, or simply wait for a given amount of time).
2. Assert Bit 9 (LOW to assert) and Bit 6 (HIGH to assert) of the core control register. This zeroes the accumulators, the serial output registers, and the serial input registers.
3. Fill the program RAM using burst-mode writes.
4. Fill the parameter RAM using burst-mode writes.
5. Assert Bit 7 of the core control register to initiate a data-memory clear sequence. Wait at least 100 µs for this sequence to complete. This bit is automatically cleared after the operation is complete.
6. Deassert Bit 9 and Bit 6 of the core control register.
7. If the newly loaded program also uses the target/slew RAM, deassert Bit 12 of the core control register to begin a volume ramp-up procedure.

## TARGET/SLEW RAM

The target/slew RAM is a bank of 64 RAM locations, each of which can each be set to autoramp from one value to a desired final value in one of four modes.

### *Summary*

The target/slew RAM is used by the DSP when a program is loaded into the program RAM that uses one or more locations in the slew RAM to access internal coefficient data. Typically, these coefficients are used for volume controls or smooth cross-fading effects, but may be used to update any value in the parameter RAM. Each of the 64 locations in the slew RAM are linked to corresponding locations in the target RAM. When a new value is written to the target RAM using the control port, the corresponding slew RAM location begins to ramp toward the target. The value is updated once per audio frame (LRCLK period).

The target RAM is 34 bits wide. The lower 28 bits contain the target data in 5.23 format for the linear and exponential (constant dB and RC-type) ramp types. For constant time ramping, the lower 28 bits contain 16 bits in 2.14 format and 12 bits to set the current step. The upper six bits are used to determine the type and speed of the ramp envelope in all modes. The format of the data write for linear and exponential formats is shown in Table 12. Table 13 shows the data write format for the constant time ramping.

In normal operation data should be written to the target/slew RAM using the safeload registers as described in the Safeload Registers section. A mute slew RAM bit is included in the core control register to simultaneously set all the slew RAM target values to 0. This is useful for implementing a global multichannel mute. When this bit is deasserted, all slew RAM values will return to their original pre-muted states.

**Table 12. Linear, Constant dB, and RC-type Ramp Data Write**

| Byte 0 | Byte 1 | Bytes 2–4 |
|---|---|---|
| 000000, curve_type[1:0] | time_const[3:0], data[27:24] | data[23:0] |

**Table 13. Constant Time Ramp Data Write**

| Byte 0 | Byte 1 | Bytes 2–4 |
|---|---|---|
| 000000, curve_type[1:0] | update_step[0], #_of_steps[2:0], data[15:12] | data[11:0], reserved[11:0] |

The four ramping curve types are

1. Linear—Value slews to target using a fixed step size.
2. Constant dB—Value slews to target using the current value to calculate the step size. The resulting curve has a constant rise and decay when measured in dB.
3. RC-type—Value slews to target using the difference between target and current values to calculate the step size, producing a simple RC type curve for rising and falling.
4. Constant Time—Value slews to the target in a fixed number of steps in a linear fashion. The control port mute has no affect on this type.

**Table 14 Target/Slew RAM Ramp Type Settings**

| Setttings | Ramp Type |
|---|---|
| 00 | Linear |
| 01 | Constant dB |
| 10 | RC-Type |
| 11 | Constant Time |

The following sections detail how the control port writes to the target/slew RAM to control the time constant and ramp type parameters.

### *Ramp Types 1–3: Linear, Constant dB, RC-type (34-Bit Write)*

The target word for the first three ramp types is broken up into three parts. The 34-bit command is written with six leading 0s to extend the data write to five bytes. The parts of the target RAM write are described below.

- Ramp Type (2 bits)
- Time Constant (4 bits)
  0000 = Fastest
  1111 = Slowest
- Data (28 Bits): 5.23 Format

### *Ramp Type 4—Constant Time (34-Bit Write)*

The target word for the constant time ramp type is written in five parts, with the 34-bit command again written with six leading zeros to extend the data write to five bytes. The parts of the constant time target RAM write are described below.

- Ramp Type (2 bits).
- Update Step (1 bit). Set to 1 when new target is loaded to trigger step value update. Value is automatically reset after the step value is updated.
- Number of Steps (3 bits). The number of steps that it takes to slew to the target value is set by these three bits, with the number of steps equal to $2^{3\text{-bit setting} + 6}$.
  000 = 64
  001 = 128
  010 = 256
  011 = 512
  100 = 1024
  101 = 2048
  110 = 4096
  111 = 8196
- Data (16 bits). 2.14 format.
- Reserved (12 bits). When writing to the RAM, these bits should all be set to 0.

### *Target and Slew RAM Initialization*

On reset, the target/slew RAM initializes to preset values. The target RAM initializes to a linear ramp type with a time constant of 5 and the data set to 1.0. The slew RAM initializes to a value of 1.0. These defaults give a full-scale (1.0 to 0.0) ramp time of 21.3 ms.

### *Linear Update Math*

Linear math is the addition or subtraction of a constant value (step). The equation to describe this step size is

$$step = \frac{2^{13}}{\frac{10^{2\times(tconst-5)}}{20}}$$

The result of the equation is normalized to a 5.23 data format. This gives a time constant range from 6.75 ms to 213.4 ms. (–60 dB relative to 0 dB full scale). An example of this kind of update is shown in

Figure 23 and Figure 24. All slew RAM figure examples, except the half-scale constant time ramp plot, show an increasing or decreasing ramp between –80 dB and 0 dB (full scale). All figures except the constant time plots (Figure 28 and Figure 29) use a time constant of 0x7 (0x0 being the fastest and 0xF being the slowest).

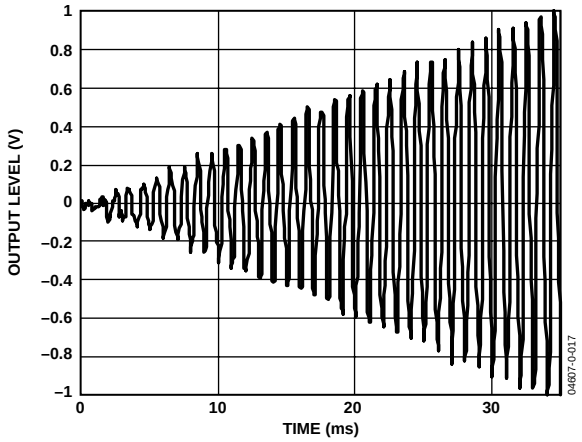


*Figure 23. Slew RAM—Linear Update Increasing Ramp*

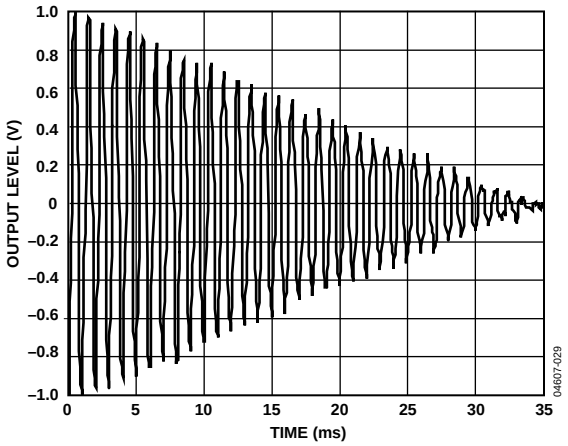


*Figure 24. Slew RAM—Linear Update Decreasing Ramp*

### *Constant dB and RC-type (Exponential) Update Math*

Exponential math is accomplished by shifts and adds with a range from 6.1 ms to 1.27 s (–60 dB relative to 0 dB full scale). When the ramp type is set to 01 (constant dB), each step size is set to the current value in the slew data. When the ramp type bits are set to 10 (RC type), the step sizes are equal to the difference between the values in the target RAM and slew RAM. Figure 25 and Figure 26 show examples of this type of target/slew RAM ramping. A decreasing ramp of both the constant dB and RC-type ramps is a mirror image of the constant dB increasing ramp, and is show in Figure 27.

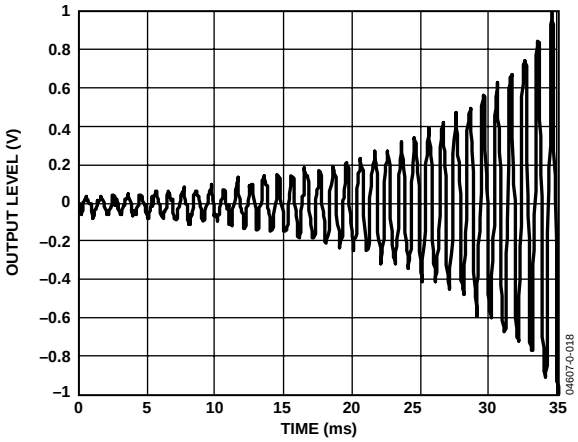


*Figure 25. Slew RAM—Constant dB Update Increasing Ramp*

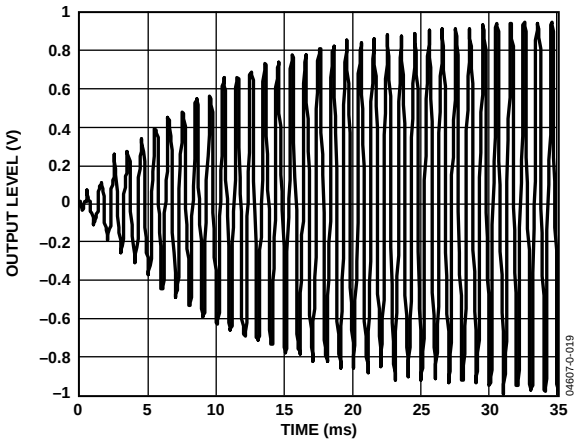


*Figure 26. Slew RAM—RC-Type Update Increasing Ramp*

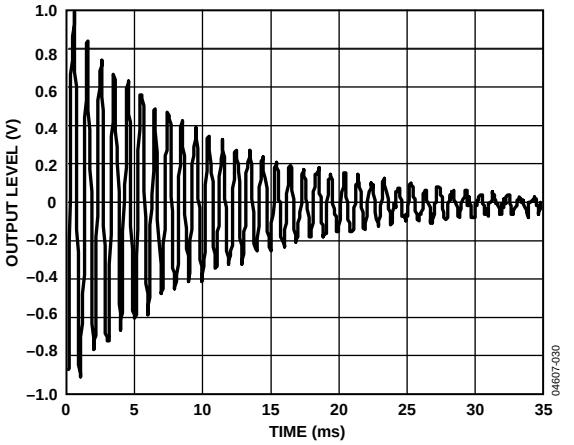


*Figure 27. Slew RAM—Constant dB and RC-Type Update Decreasing Ramp, Full Scale*

### *Constant Time Update Math*

Constant time math is accomplished by adding a step value that is calculated after each new target is loaded. The equation for this step size is

$$Step = (Target\ Data - Slew\ Data)/(Number\ of\ Steps)$$

Figure 28 shows a plot of the target/slew RAM operating in constant time mode. For this example, 128 steps are used to reach the target value. This type of ramping will take a fixed amount of time for a given number of steps, regardless of the difference in the initial state and the target value. Figure 29 shows a plot of a constant time ramp from –80 dB to –6 dB (half scale) using 128 steps. You can see that the ramp takes the same amount of time as the previous ramp from –80 dB to 0 dB. A constant time decreasing ramp plot is shown in Figure 29.

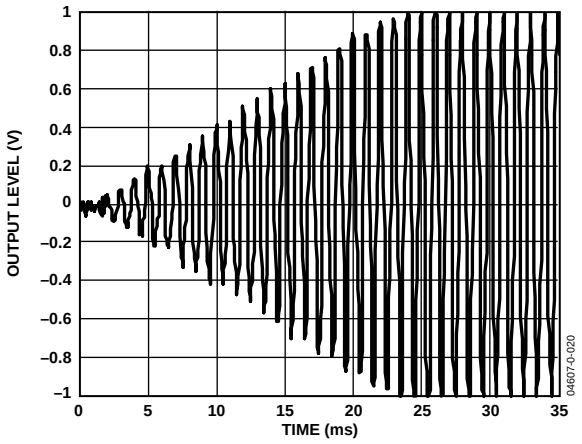


*Figure 28. Slew RAM—Constant Time Update Increasing Ramp, Full Scale*

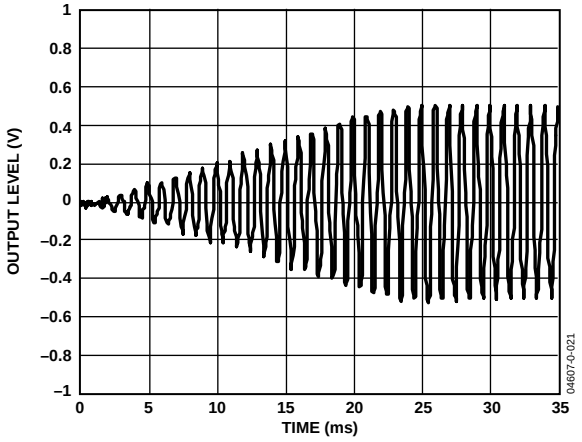


*Figure 29. Slew RAM—Constant Time Update Increasing Ramp, Half Scale*

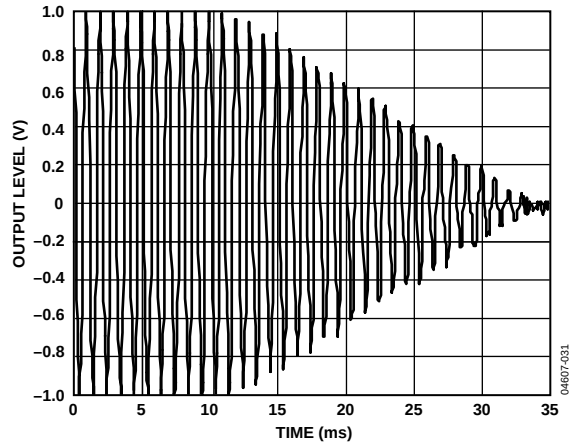


*Figure 30. Slew RAM—Constant Time Update Decreasing Ramp, Full Scale*

## SAFELOAD REGISTERS

Many applications require real-time control of signal processing parameters, such as filter coefficients, mixer gains, multichannel virtualizing parameters, or dynamics processing curves. To prevent instability from occurring, all of the parameters of a biquad filter must be updated at the same time. Otherwise, the filter could execute for one or two audio frames with a mix of old and new coefficients. This mix could cause temporary instability, leading to transients that could take a long time to decay. To eliminate this problem, the ADAU1421 loads a set of 10 registers in the control port (five for 28-bit parameters, and another five for indirectly addressing the target/slew RAMs) with the desired parameter or target/slew RAM address and data. Five registers are used because a biquad filter uses five coefficients, and it is desirable to be able to do a complete biquad update in one transaction. The safeload registers can be used to update either the parameter RAM or target/slew RAM values. Once these registers are loaded, the appropriate initiate safe transfer bit (there are separate bits for parameter and target/slew loads) in the core control register should be set to initiate the loading into RAM. Program lengths should be limited to 2555 cycles (2560 − 5) to ensure that the ADAU1421 is able to perform the safeloads. It can be guaranteed that the safeload will have occurred within one LRCLK period (21 µs at $f_s$ = 48 kHz) of the initiate safe transfer bit being set.

The safeload logic automatically sends only those safeload registers that have been written to since the last safeload operation. For example, if only two parameters are to be sent, only two of the five safeload registers must be written to. When the initiate safe transfer bit (in the core control register) is asserted, only those two registers are sent; the other three registers are not sent to the RAM and can still hold old or invalid data.

**Table 15. Data Capture Control Registers**

| Register Bits | Function |
|---|---|
| 13:2 | 12-Bit Program Counter Address |
| 1:0 | Register Select<br>00 = Mult_X_input<br>01 = Mult_Y_input<br>10 = MAC_output<br>11 = Accum_fback |

## DATA CAPTURE REGISTERS

The ADAU1421's data capture feature allows the data at any node in the signal processing flow to be sent to one of six control port-readable registers or to a serial output pin. This can be used to monitor and display information about internal signal levels or compressor/limiter activity.

The ADAU1421 contains six independent control port-readable data capture registers, and two digital output capture registers. These registers are useful when debugging the signal processing flow.

For each of the data capture registers, a capture count and a register select must be set. The capture count is a number between 0 and 2559 that corresponds to the program step number where the capture will occur. The register select field programs one of four registers in the DSP core that will be transferred to the data capture register when the program counter equals the capture count. The register select field selections are shown in Table 16.

**Table 16. Data Capture Output Register Select**

| Settings | Register |
|---|---|
| 00 | Multiplier X Input (Mult_X_input) |
| 01 | Multiplier Y Input (Mult_Y_input) |
| 10 | Multiplier-Accumulator Output (MAC_out) |
| 11 | Accumulator Feedback (Accum_fback) |

The capture count and register select bits are set by writing to one of the eight data capture registers at register addresses

4170: Control Port Data Capture Setup Register 0
4171: Control Port Data Capture Setup Register 1
4172: Control Port Data Capture Setup Register 2
4173: Control Port Data Capture Setup Register 3
4174: Control Port Data Capture Setup Register 4
4175: Control Port Data Capture Setup Register 5
4176: Digital Out Data Capture Setup Register 0
4177: Digital Out Data Capture Setup Register 1

The captured data is in 5.19 twos complement data format for all eight register select fields. The four LSBs are truncated from the internal 5.23 data-word.

The data that must be written to set up the data capture is a concatenation of the 12-bit program count index with the 2-bit register select field. The capture count and register select values that correspond to the desired point to be monitored in the signal processing flow can be found in a file output from the program compiler. The capture registers can be accessed by reading from locations 4170–4175 (0x104A–0x104F) (for control port capture registers). The format for reading and writing to the data capture registers can be seen in Table 23 and Table 24

## AUDIO CORE CONTROL REGISTER

The controls in this register set the operation of the ADAU1421's DSP core. Bits 6 to 9 can be set to initiate a shutdown of the core. The output is muted when this is performed, so it is best to first assert bit 12 of the Audio Core Control Register (if slew RAM locations are used as volume controls in the program) to avoid a click or pop when shutdown is asserted. Bit 13 indicates when this operation is complete.

### *Slew RAM Muted (Bit 13)*

This bit is set to 1 when the slew RAM mute operation has been completed. This bit is read-only and is automatically cleared by reading.

### *Write Zero to Target RAM (Bit 12)*

Setting this bit to 1 is equivalent to writing zeros to all locations in the Target RAM. The RAM will then slew to zero muting the volume. The bit should be cleared to zero to enable normal operation.

### *Use Serial Out LRCLK for Output Latch (Bit 10)*

Normally, data is transferred from the DSP core to the serial output registers at the end of each program cycle. In some cases (e.g., when output sample rate is set to some multiple of input sampling rate), it is desirable to transfer the internal core data multiple times during a single input audio sample period. Setting this bit to 1 allows the output LRCLK signal to control this data transfer rather than the internal end-of-sequence signal. Operation in this mode may require custom assembly-language coding in the ADI graphical tools.

### *Clear Registers to All Zeros (Bit 9)*

Setting this bit to 0 sets the contents of the accumulators and serial output registers to 0. Like the other register bits, this one powers up to 0. This means the AD1940/AD1941 power up in clear mode and will not pass a signal until a 1 is written to this bit. This is intended to prevent noises from inadvertently occurring during the power-up sequence.

### *Force Multiplier to Zero (Bit 8)*

When this bit is set to 1, the input to the DSP multiplier is set to 0, which results in the multiplier output being 0. This control bit is included for maximum flexibility, and is normally not used.

### *Initialize Data Memory with Zeros (Bit 7)*

Setting this bit to 1 initializes all data memory locations to 0. This bit is cleared to 0 after the operation is complete. This bit should be asserted after a complete program/parameter download has occurred to ensure click-free operation.

### *Zero Serial Input Port (Bit 6)*

When this bit is set to 1, the serial input channels are forced to all 0s. and effectively muted.

### *Initiate Safe Transfer to Target RAM (Bit 5)*

Setting this bit to 1 initiates a safeload transfer to the target/slew RAM. This bit clears when the operation is completed. Of five safeload register pairs (address/data), only those registers that have been written since the last safeload event are transferred. Address 0 corresponds to the first target RAM location.

### *Initiate Safe Transfer to Parameter RAM (Bit 4)*

Setting this bit to 1 initiates a safeload transfer to the parameter RAM. This bit clears when the operation is completed. Of five safeload registers pairs (address/data), only those registers that have been written since the last safeload event are transferred. Address 0 corresponds to the first parameter RAM location.

### *Input Serial Port to Sequencer Sync (Bits 3:2)*

Normally, the internal sequencer is synchronized to the incoming audio frame rate by comparing the internal program counter with the edge of the LRCLK input signal. In some cases the AD1940/AD1941 may be used to decimate an incoming signal by some integer factor. In this case, it is desirable to synchronize the sequencer to a submultiple of the incoming

LRCLK rate so more than one audio input sample is available to the program during a single audio output frame. For example, if these bits are set to 01 (LRCLK/2), a 96 kHz input can be used with a 48 kHz output, allowing two consecutive input samples to be processed during a single audio output frame. Operation in this mode may require custom assembly-language coding in the ADI graphical tools.

### *Program Length (Bits 1:0)*

**96 kHz and 192 kHz modes**

These bits set the length of the internal program. The default program length is 2560 instructions for $f_s$ = 48 kHz, but the program length can be shortened by factors of 2 to accommodate sample rates higher than 48 kHz. For $f_s$ = 96 kHz the program length should be set to 1280 (01), and the length should be set at 640 steps (10) for $f_s$ = 192 kHz.

**Low Power Modes**

All the blocks in the ADAU1421 are individually controlled by Power-up bits. Following a reset all the bits are zero indicating that the blocks are all powered down. Blocks can be powered up individually by setting the appropriate bit in the Power Control Register.

## RAM CONFIGURATION REGISTER

The ADAU1421 use a modulo RAM addressing scheme to allow filters and other blocks to be coded easily without requiring filter data to be explicitly moved during the filtering operation. This is accomplished by adding the contents of an address offset counter to the actual base address supplied in the ADAU1421's core. This address offset counter is incremented automatically at the audio frame rate.

This method works well for most audio applications that involve filtering. In some cases, however, it is desirable to have direct access to the RAM, bypassing the autoincrementing address offset counter. For this reason, the data memories in the ADAU1421 can be divided into modulo and nonmodulo portions by programming the RAM Modulo Control Register (Table 31). The address range from 0 to 512 × (RAM configuration register contents) is treated as modulo memory with autoincrementing address offset registers. The maximum setting of this register is the full size of the RAM, or 6,144 (6 k) data words. Note that addresses in this range automatically wrap around the modulo boundary as set by the register. This feature is not normally used with ADI-supplied blocks. For normal operation, this register may be left in its default state, which sets up the entire RAM to use the autoincrement feature. This feature is included for maximum programming flexibility and may be used in the case of special software development.

## CONTROL PORT READ/WRITE DATA FORMATS

The read/write formats of the control port are designed to be byte-oriented. This allows for easy programming of common microcontroller chips. In order to fit into a byte-oriented format, 0s are appended to the data fields before the MSB in order to extend the data word to the next multiple of eight bits. For example, 28-bit words written to the parameter RAM are appended with four leading 0s in order to reach 32 bits (4 bytes); 40-bit words written to the program RAM are not appended with any 0s because it is already a full 5 bytes. These zero-extended data fields are appended to a 3-byte field consisting of a 7-bit chip address, a read/write bit, and an 11-bit RAM/register address. The control port knows how many data bytes to expect based on the address that is received in the first three bytes.

The total number of bytes for a single-location write command can vary from four bytes (for a control register write), to eight bytes (for a program RAM write). Burst mode may be used to fill contiguous register or RAM locations. A burst mode write is done by writing the address and data of the first RAM/register location to be written. Rather than ending the control port transaction the next data word can be written immediately without first writing its specific address. The ADAU1421 control ports autoincrement the address of each write, even across the boundaries of the different RAMs and registers.

**Table 17. Parameter RAM Read/Write Format (Single Address)**

| Byte 0 | Byte 1 | Byte 2 | Byte 3 | Bytes 4–6 |
|---|---|---|---|---|
| chip_adr [6:0], $\overline{W}$/R | 000, param_adr [12:8] | param_adr [7:0] | 0000, param [27:24] | param [23:0] |

**Table 18. Parameter RAM Block Read/Write Format (Burst Mode)**

| Byte 0 | Byte 1 | Byte 2 | Byte 3 | Bytes 4–6 | Byte 7 | Byte 11 |
|---|---|---|---|---|---|---|
| chip_adr [6:0], $\overline{W}$/R | 000, param_adr [12:8] | param_adr [7:0] | 0000, param [27:24] | Param [23:0] | Byte 8 | Byte 12 |
| | | | | | Byte 9 | Byte 13 |
| | | | | | Byte 10 | Byte 14 |
| | | | <—param_adr—> | | param_adr + 1 | param_adr + 2 |

**Table 19. Program RAM Read/Write Format (Single Address)**

| Byte 0 | Byte 1 | Byte 2 | Bytes 3–7 |
|---|---|---|---|
| Chip_adr [6:0], $\overline{W}$/R | 000, prog_adr [12:8] | prog_adr [7:0] | prog [39:0] |

**Table 20. Program RAM Block Read/Write Format (Burst Mode)**

| Byte 0 | Byte 1 | Byte 2 | Byte 3-7 | Byte 8 | Byte 13 |
|---|---|---|---|---|---|
| chip_adr [6:0], $\overline{W}$/R | 000, prog_adr [12:8] | prog_adr [7:0] | Prog [39:0] | Byte 9 | Byte 14 |
| | | | | Byte 10 | Byte 15 |
| | | | | Byte 11 | Byte 16 |
| | | | | Byte 12 | Byte 17 |
| | | | <—prog_adr—> | prog_adr +1 | prog_adr +2 |

**Table 21. Control Register Read/Write Format (Core, Serial Out 0, Serial Out 1)**

| Byte 0 | Byte1 | Byte 2 | Byte 3 | Byte 4 |
|---|---|---|---|---|
| chip_adr [6:0], $\overline{W}$/R | 000, reg_adr [12:8] | reg_adr [7:0] | data [15:8] | data [7:0] |

**Table 22. Control Register Read/Write Format (RAM Configuration, Serial Input)**

| Byte 0 | Byte1 | Byte 2 | Byte 3 |
|---|---|---|---|
| chip_adr [6:0], $\overline{W}$/R | 000, reg_adr [12:8] | reg_adr [7:0] | data [7:0] |

**Table 23. Data Capture Register Write Format**

| Byte 0 | Byte 1 | Byte 2 | Byte 3 | Byte 4 |
|---|---|---|---|---|
| chip_adr [6:0], $\overline{W}$/R | 000, data_capture_adr [12:8] | data_capture_adr [7:0] | 000, progCount [10:6][1] | progCount [5:0][1], regSel [1:0][2] |

**Table 24. Data Capture (Control Port Readback) Register Read Format**

| Byte 0 | Byte 1 | Byte 2 | Bytes 3–5 |
|---|---|---|---|
| chip_adr [6:0], $\overline{W}$/R | 000, data_capture_adr [12:8] | data_capture_adr [7:0] | data [23:0] |

**Table 25. Safeload Register Data Write Format**

| Byte 0 | Byte 1 | Byte 2 | Byte 3 | Bytes 4–7 |
|---|---|---|---|---|
| chip_adr [6:0], $\overline{W}$/R | 000, safeload_adr [12:8] | safeload_adr [7:0] | 000000, data [33:32] | data [31:0] |

**Table 26. Safeload Register Address Write Format**

| Byte 0 | Byte 1 | Byte 2 | Byte 3 | Byte 4 |
|---|---|---|---|---|
| chip_adr [6:0], $\overline{W}$/R | 000, safeload_adr [12:8] | safeload_adr [7:0] | 000000, param_adr [9:8] | param_adr [7:0] |

# SERIAL DATA INPUT/OUTPUT PORTS

The ADAU1421's flexible serial data input and output ports can be set to accept or transmit data in 2-channel formats or in an 8- or 16-channel TDM stream. Data is processed in twos complement, MSB-first format. The left channel data field always precedes the right channel data field in the 2-channel streams. In the TDM modes, Slots 0 to 3 (8-channel TDM) or Slots 0 to 7 (16-channel TDM) fall in the first half of the audio frame, and Slots 4 to 7 (or Slots 8 to 15 in 16-channel TDM) are in the second half of the frame. The serial modes are set in the serial output and serial input control registers.

The input serial port is synchronized with the output serial port, i.e. BCLK1 and LRCLK1 are used for both. The output serial port can be programmed to be a master or a slave port.

The input control register allows control of clock polarity and data input modes. The valid data formats are I²S , left-justified, right-justified (24-, 20-, 18-, or 16-bit), 8-channel, and 16-channel TDM. In all modes except for the right-justified modes, the serial port will accept an arbitrary number of bits up to a limit of 24. Extra bits will not cause an error, but they will be truncated internally. Proper operation of the right-justified modes requires that there be exactly 64 BCLKs per audio frame.

The LRCLK in TDM mode can be input to the ADAU1421 as either a 50/50 duty cycle clock or as a bit-wide pulse.

The two clock domains on the serial output ports can generate two separate 8-channel TDM streams or one 16-channel TDM stream. When in 16-channel TDM mode, the data is clocked by LRCLK1 and BCLK1. The ADAU1421 must be in slave mode for 16-channel TDM unless the data is sampled at 48 kHz; the part cannot generate a TDM bit clock that is fast enough to support 96 kHz or 192 kHz. In 8-channel TDM mode, the ADAU1421 can be a master for 48 kHz and 96 kHz data, but not for 192 kHz data. Table 27 displays the modes in which the serial output port will function.

The output control registers give the user control of clock polarities, clock frequencies, clock types, and data format. In all modes except for the right-justified modes (MSB delayed by 8, 12, or 16), the serial port accepts an arbitrary number of bits up to a limit of 24. Extra bits will not cause an error, but will be truncated internally. Proper operation of the right-justified modes requires the LSB to align with the edge of the LRCLK. The default settings of all serial port control registers correspond to 2-channel I²S mode. LRCLK1 and BCLK1 are clocks for Serial Output Port.

All registers default to being set as all 0s. All register settings apply to both master and slave modes unless otherwise noted.

Table 28 shows the proper configurations for standard audio data formats.

**Table 27 Serial Output Port Master/Slave Mode Capabilities**

| $f_s$ | 2-Channel Modes (I²S, Left-Justified, Right-Justified) | 8-Channel TDM | 16-Channel TDM |
|---|---|---|---|
| 48 kHz | Master and slave | Master and slave | Master and slave |
| 96 kHz | Master and slave | Master and slave | Slave only |
| 192 kHz | Master and slave | Slave only | Slave only |

**Table 28. Data Format Configurations**

| Format | LRCLK Polarity | LRCLK Type | BCLK Polarity | MSB Position |
|---|---|---|---|---|
| I²S (Figure 31) | Frame begins on falling edge | Clock | Data changes on falling edge | Delayed from LRCLK edge by one BCLK |
| Left-Justified (Figure 32) | Frame begins on rising edge | Clock | Data changes on falling edge | Aligned with LRCLK edge |
| Right-Justified (Figure 33) | Frame begins on rising edge | Clock | Data changes on falling edge | Delayed from LRCLK edge by 8, 12, or 16 BCLKs |
| TDM with Clock (Figure 34) | Frame begins on falling edge | Clock | Data changes on falling edge | Delayed from start of word clock by one BCLK |
| TDM with Pulse (Figure 35) | Frame begins on rising edge | Pulse | Data changes on falling edge | Delayed from start of word clock by one BCLK |

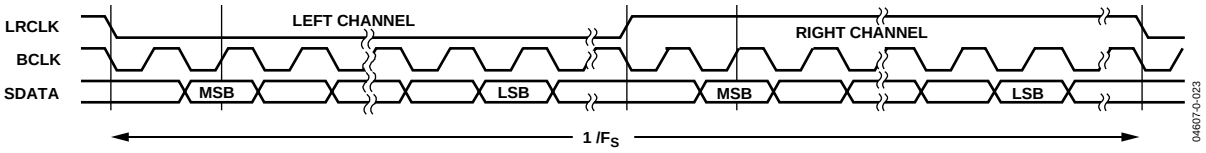


*Figure 31. I²S Mode—16 to 24 Bits per Channel*

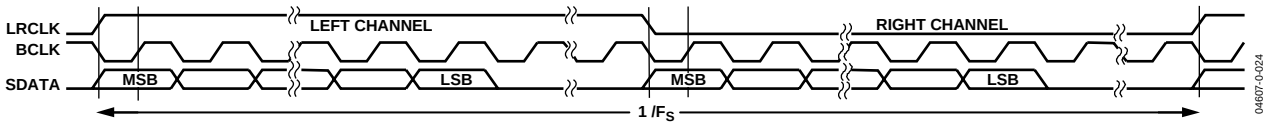


*Figure 32. Left-Justified Mode—16 to 24 Bits per Channel*

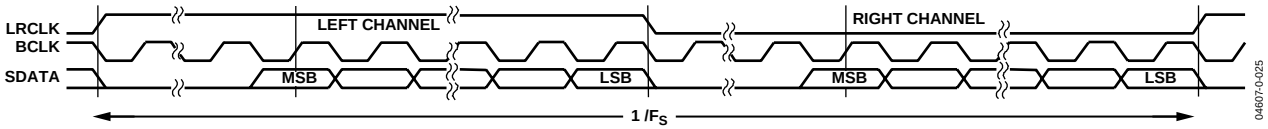


*Figure 33. Right-Justified Mode—16 to 24 Bits per Channel*

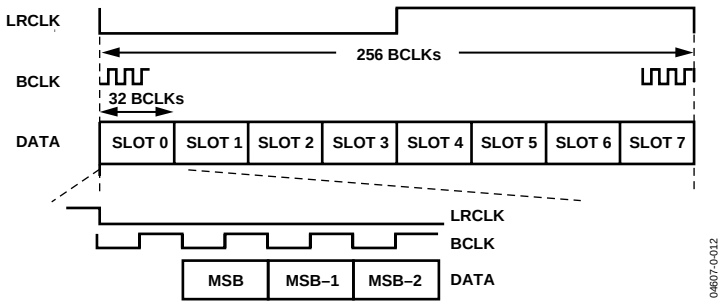


*Figure 34. 8-Channel TDM Mode. This diagram shows just one of the formats in which the ADAU1421 can operate in TDM mode. Please refer to the Serial Data Input/Output Ports section for a more complete description of the modes of operation.*

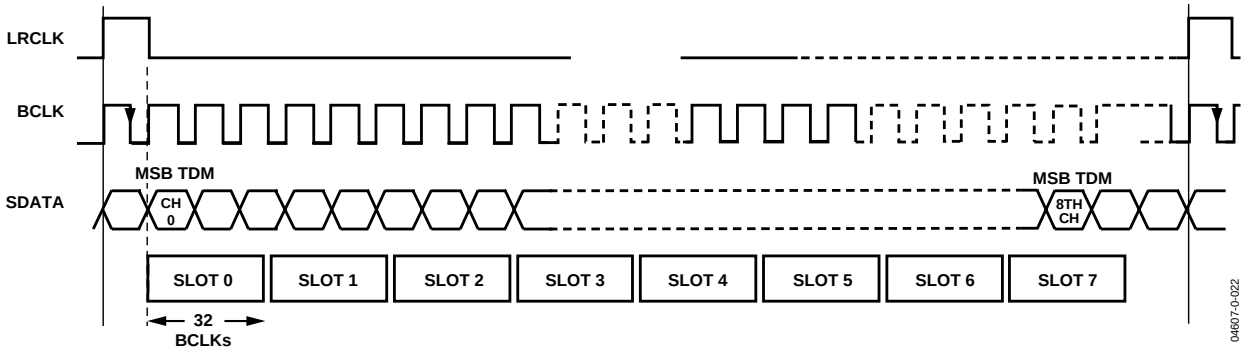


*Figure 35. TDM Mode with Pulse Word Clock*

# CONTROL REGISTERS

**Table 29 Audio Register Map**

| Register Address (Hex) | Register Name | Register Width (Bits) |
|---|---|---|
| 1052 | Audio Core Control Register | 16 |
| 1053 | RAM Modulo Control Register | 8 |
| 1054 | Serial Output Control Register | 16 |
| 1055 | Serial Input Control Register | 8 |
| 1056 | SRC Serial Port Control Register | 8 |
| 1057 | ADC Input MUX Control Register | 16 |
| 1058 | Power Control Register | 16 |
| 1059 | User Control Register 1 | 16 |
| 105A | User Control Register 2 | 16 |

**Table 30 Audio Core Control Register**

| Register Address 0x1052 | Default = 0x0000 |
|---|---|
| **Register bits** | **Function** |
| 15 | Reserved (Set to 0) |
| 14 | Enable SDO2 and SDO3<br>0 = Disabled<br>1 = Enabled |
| 13 | (Read only) Indicates when slew ram is muted |
| 12 | Equivalent to writing 0's to the target RAM<br>0 = Normal Operation<br>1 = RAM Zeroed |
| 11 | Reserved (Set to 0) |
| 10 | LRCLK used for output serial data transfer<br>0 = Disabled<br>1 = Enabled |
| 9 | Clears internal processor registers (active low)<br>0 = Registers Cleared<br>1 = Normal Operation |
| 8 | Forces multiplier input to zero<br>0 = Normal Operation<br>1 = Force Zero |
| 7 | Initialises data RAM to zero<br>0 = Normal Operation<br>1 = Enabled |
| 6 | Mute serial input ports<br>0 = Normal Operation<br>1 = Muted |
| 5 | Initiate safeload to target\slew RAM<br>0 = Off<br>1 = On |
| 4 | Initiate safeload to parameter RAM<br>0 = Off<br>1 = On |
| 3 : 2 | Determines the input SPORT to program sequencer ratio<br>00 – LRCLK<br>01 – LRCLK\2<br>10 – LRCLK\4<br>11 – LRCLK\8 |
| 1 : 0 | Program Length<br>00 – 2560 (48K)<br>01 – 1280 (96K Digital IO only)<br>10 – 640 (192K Digital IO only)<br>11 – Reserved |

**Table 31 RAM Modulo Control Register (8 bits)**

| Register Address 0x1053 | Default = 0x28 |
|---|---|
| **Register bits** | **Function** |
| 7 : 6 | Reserved (Set to 0) |
| 5 : 0 | Ram Modulo Size (1 LSB – 512 locations) |

**Table 32 Serial Output Control Register**

| Register Address 0x1054 | Default = 0x0000 |
|---|---|
| **Register bits** | **Function** |
| 15 | Dither Enable<br>0 = Disabled<br>1 = Enabled |
| 14 | Enables 16 bit TDM mode<br>0 = 8 channel TDM<br>1 = 16 channel TDM |
| 13 | LRCLK Polarity<br>0= Left low, Right high<br>1 = Left high, Right low |
| 12 | BCLK Polarity<br>0 = Data changes on falling edge<br>1 = Data changes on rising edge |
| 11 | Master/Slave mode select<br>0 = Slave<br>1 = Master |
| 10 : 9 | BCLK Frequency (Master mode)<br>00 = 3.072MHz (48K)<br>01 = 6.144MHz (96K Digital IO only)<br>10 = 12.288MHz (192K Digital IO only)<br>11 = Reserved |
| 8 : 7 | LRCLK Frequency (Master Mode)<br>00 = 48K<br>01 = 96K<br>10 = 192K<br>11 = Reserved |
| 6 | Frame Sync Type<br>0 = LRCLK<br>1 = Pulse |
| 5 | TDM Enable<br>0 = Serial Data Out<br>1 = TDM Out |
| 4 : 2 | MSB Position<br>000 = Delay by 1<br>001 = Delay by 0<br>010 = Delay by 8<br>011 = Delay by 12<br>100 = Delay by 16<br>All others are reserved |
| 1: 0 | Wordlength<br>00 = 24 bits<br>01 = 20 bits<br>10 = 16 bits<br>11 = 16 bits |

**Table 33 Serial Input Control Register (8 bits)**

| Register Address 0x1055 | Default = 0x00 |
|---|---|
| **Register bits** | **Function** |
| 7 : 6 | Reserved (Set to 0) |
| 5 | 16 bit TDM mode<br>0 = 8 channel TDM<br>1 = 16 channel TDM |
| 4 | LRCLK Polarity<br>0 = Left low, Right high<br>1 = Left high, Right low |
| 3 | BCLK Polarity<br>0 = Data changes on falling edge<br>1 = Data changes on rising edge |
| 2 : 0 | Serial Input mode<br>000 = I2S<br>001 = Left Justified<br>010 = 8 ch TDM<br>011 = Right Justified, 24 bit<br>100 = Right Justified, 20 bit<br>101 = Right Justified, 18 bit<br>110 = Right Justified, 16 bit<br>All others are reserved |

**Table 34 SRC Serial Port Control Register (8 bits)**

| Register Address 0x1056 | Default = 0x00 |
|---|---|
| **Register bits** | **Function** |
| 7 | Reserved (Set to 0) |
| 6 : 5 | SRC Serial Input Port Select<br>00 = SDIN3<br>01 = SDIN2<br>10 = SDIN1<br>11 = SDIN0 |
| 4 | LRCLK Polarity<br>0 = Left low, Right high<br>1 = Left high, Right low |
| 3 | BCLK Polarity<br>0 = Data changes on falling edge<br>1 = Data changes on rising edge |
| 2 : 0 | Serial Input mode<br>000 = I2S<br>001 = Left Justified<br>010 = 8 ch TDM<br>011 = Right Justified, 24 bit<br>100 = Right Justified, 20 bit<br>101 = Right Justified, 18 bit<br>110 = Right Justified, 16 bit<br>All others are reserved |

**Table 35 ADC Input MUX Control Register**

| Register Address 0x1057 | Default = 0x0001 |
|---|---|
| **Register bits** | **Function** |
| 15 : 4 | Reserved (Set to 0) |
| 3 | AIN4 to ADC |
| 2 | AIN3 to ADC |
| 1 | AIN2 to ADC |
| 0 | AIN1 to ADC |

**Table 36 Power Control Register**

| Register Address 0x1058 | Default = 0x0000 |
|---|---|
| **Register bits** | **Function** |
| | 0 = Powered Down – 1 = Powered Up |
| 15 | PLL |
| 14 | Reference Buffer |
| 13 | ADC |
| 12 | VOUT4 DAC |
| 11 | VOUT3 DAC |
| 10 | VOUT2 DAC |
| 9 | VOUT1 DAC |
| 8 | AUX2 Right DAC |
| 7 | AUX2 Left DAC |
| 6 | AUX1\HP Right DAC |
| 5 | AUX1\HP Left DAC |
| 4 | Headphone Amplifier Right |
| 3 | Headphone Amplifer Left |
| 2 | SRC |
| 1 | Digital ADC and DAC engine |
| 0 | Audio Processor |

**Table 37 User Control Register 1**

| Register Address 0x1059 | Default = 0x0000 |
|---|---|
| **Register bits** | **Function** |
| 15 : 13 | Reserved (Set to 0) |
| 12 : 9 | Disable Test Mode<br>These bits are zero by default. Setting the bits to 0b1111 will disable the test mode and pins TEST3 to TEST6 will become static. |
| 8 | SRC Mux Enable<br>0 = Disabled<br>1 = Enabled |
| 7 | (Read only) Indicates SRC is locked<br>0 = SRC Not Locked<br>1 = SRC Locked |
| 6 | Enables MCLK out pin<br>0 = MCLKO pin disabled<br>1 = MCLKO pin enabled |
| 5 : 3 | MCLKO select<br>000 = Reserved<br>001 = ADC and DAC digital engine clock<br>010 = Reserved<br>011 = Reserved<br>1xx = ADC and DAC clock |
| 2 : 1 | PLL Clock Select<br>00 – 64 x $f_S$ (3.072 MHz)<br>01 – 128 x $f_S$ (6.144 MHz)<br>10 – 256 x $f_S$ (12.288 MHz)<br>11 – 512 x $f_S$ (24.576 MHz) |
| 0 | Enable PLL<br>0 = PLL Bypassed<br>1 = PLL In Use |

**Table 38 User Control Register 2**

| Register Address 0x105A | | |
|---|---|---|
| **Register bits** | **Function** | **Default = 0x0000** |
| 15 : 8 | Reserved (Set to 0) | |
| 7 | Headphone Amplifier Mute<br>0 = Normal Operation<br>1 = Mute | |
| 6 | Headphone Amplifier Short-Circuit Protection<br>0 = Disabled<br>1 = Enabled | |
| 5 | Headphone Amplifier Three-State<br>0 = Normal Operation<br>1 = Three-state | |
| 4 : 0 | Headphone Amplifier Attenuation<br>00000 = 0 dB<br>00001 = -1.5 dB<br>00010 = -3.0 dB<br>11110 = -45.0 dB<br>11111 = -46.5 dB | |

# TYPICAL APPLICATION DIAGRAM

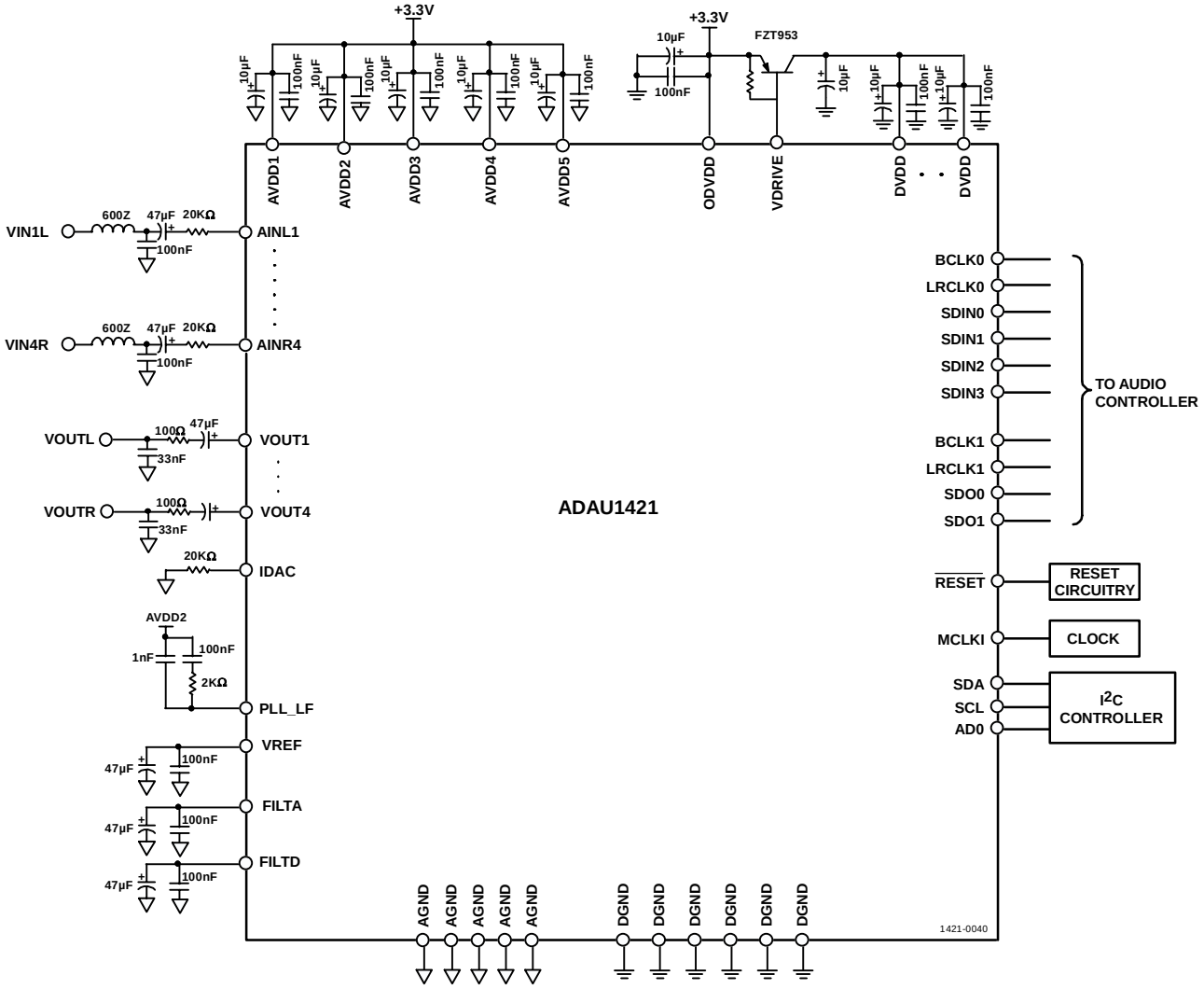


*Figure 36. Typical Application Circuit*

# OUTLINE DIMENSIONS

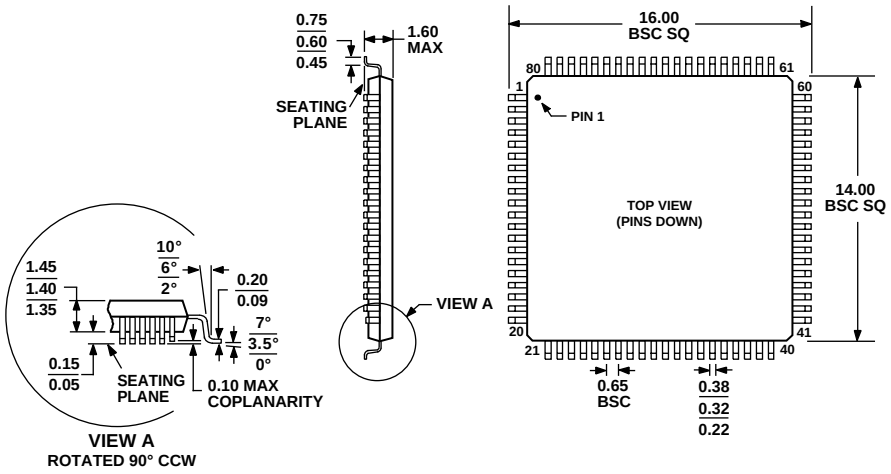


*Figure 37. 80-Lead Low Profile Quad Flat Package [LQFP]*
*(ST-80-2)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option |
|---|---|---|---|
| ADAU1421YSTZ[1] | -40°C to +105°C | Low Profile Quad Flat Package (LQFP) | ST-80-2 |

[1] Z = Pb-free part.

The ADAU1421 is a Pb-free environmentally friendly product. It is manufactured using the most up-to-date materials and processes. The coating on the leads of each device is 100% pure Sn electroplate. The device is suitable for Pb-free applications, and can withstand surface-mount soldering at up to 255°C (±5°C).

In addition, it is backward-compatible with conventional SnPb soldering processes. This means the electroplated Sn coating can be soldered with Sn/Pb solder pastes at conventional reflow temperatures of 220°C to 235°C.

## NOTES


PR05621–0–6/05(PrD)